chapter

3

Methods of Analysis

No great work is ever done in a hurry. To develop a great scientific discovery, to print a great picture, to write an immortal poem, to become a minister, or a famous general—to do anything great requires time, patience, and perseverance. These things are done by degrees, "little by little."

—W. J. Wilmont Buxton

Enhancing Your Career

Career in Electronics

One area of application for electric circuit analysis is electronics. The term *electronics* was originally used to distinguish circuits of very low current levels. This distinction no longer holds, as power semiconductor devices operate at high levels of current. Today, electronics is regarded as the science of the motion of charges in a gas, vacuum, or semiconductor. Modern electronics involves transistors and transistor circuits. The earlier electronic circuits were assembled from components. Many electronic circuits are now produced as integrated circuits, fabricated in a semiconductor substrate or chip.

Electronic circuits find applications in many areas, such as automation, broadcasting, computers, and instrumentation. The range of devices that use electronic circuits is enormous and is limited only by our imagination. Radio, television, computers, and stereo systems are but a few.

An electrical engineer usually performs diverse functions and is likely to use, design, or construct systems that incorporate some form of electronic circuits. Therefore, an understanding of the operation and analysis of electronics is essential to the electrical engineer. Electronics has become a specialty distinct from other disciplines within electrical engineering. Because the field of electronics is ever advancing, an electronics engineer must update his/her knowledge from time to time. The best way to do this is by being a member of a professional organization such as the Institute of Electrical and Electronics Engineers (IEEE). With a membership of over 300,000, the IEEE is the largest professional organization in the world. Members benefit immensely from the numerous magazines, journals, transactions, and conference/symposium proceedings published yearly by IEEE. You should consider becoming an IEEE member.

Troubleshooting an electronic circuit board.
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3.1 Introduction

Having understood the fundamental laws of circuit theory (Ohm's law and Kirchhoff's laws), we are now prepared to apply these laws to develop two powerful techniques for circuit analysis: nodal analysis, which is based on a systematic application of Kirchhoff's current law (KCL), and mesh analysis, which is based on a systematic application of Kirchhoff's voltage law (KVL). The two techniques are so important that this chapter should be regarded as the most important in the book. Students are therefore encouraged to pay careful attention.

With the two techniques to be developed in this chapter, we can analyze any linear circuit by obtaining a set of simultaneous equations that are then solved to obtain the required values of current or voltage. One method of solving simultaneous equations involves Cramer's rule, which allows us to calculate circuit variables as a quotient of determinants. The examples in the chapter will illustrate this method; Appendix A also briefly summarizes the essentials the reader needs to know for applying Cramer's rule. Another method of solving simultaneous equations is to use *MATLAB*, a computer software discussed in Appendix E.

Also in this chapter, we introduce the use of *PSpice for Windows*, a circuit simulation computer software program that we will use throughout the text. Finally, we apply the techniques learned in this chapter to analyze transistor circuits.

3.2 Nodal Analysis

Nodal analysis is also known as the *node-voltage method*.

Nodal analysis provides a general procedure for analyzing circuits using node voltages as the circuit variables. Choosing node voltages instead of element voltages as circuit variables is convenient and reduces the number of equations one must solve simultaneously.

To simplify matters, we shall assume in this section that circuits do not contain voltage sources. Circuits that contain voltage sources will be analyzed in the next section.

In *nodal analysis*, we are interested in finding the node voltages. Given a circuit with n nodes without voltage sources, the nodal analysis of the circuit involves taking the following three steps.

Steps to Determine Node Voltages:

1. Select a node as the reference node. Assign voltages v_1, $v_2, \dots, v_{n-1}$ to the remaining $n - 1$ nodes. The voltages are referenced with respect to the reference node.
2. Apply KCL to each of the $n - 1$ nonreference nodes. Use Ohm's law to express the branch currents in terms of node voltages.
3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

We shall now explain and apply these three steps.

The first step in nodal analysis is selecting a node as the *reference* or *datum node*. The reference node is commonly called the *ground* since it is assumed to have zero potential. A reference node is indicated by any of the three symbols in Fig. 3.1. The type of ground in Fig. 3.1(c) is called a *chassis ground* and is used in devices where the case, enclosure, or chassis acts as a reference point for all circuits. When the potential of the earth is used as reference, we use the *earth ground* in Fig. 3.1(a) or (b). We shall always use the symbol in Fig. 3.1(b).

Once we have selected a reference node, we assign voltage designations to nonreference nodes. Consider, for example, the circuit in Fig. 3.2(a). Node 0 is the reference node ($v = 0$), while nodes 1 and 2 are assigned voltages v_1 and v_2, respectively. Keep in mind that the node voltages are defined with respect to the reference node. As illustrated in Fig. 3.2(a), each node voltage is the voltage rise from the reference node to the corresponding nonreference node or simply the voltage of that node with respect to the reference node.

The number of nonreference nodes is equal to the number of independent equations that we will derive.

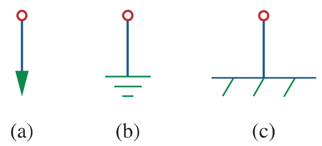


Figure 3.1
Common symbols for indicating a reference node, (a) common ground, (b) ground, (c) chassis ground.

As the second step, we apply KCL to each nonreference node in the circuit. To avoid putting too much information on the same circuit, the circuit in Fig. 3.2(a) is redrawn in Fig. 3.2(b), where we now add i_1, i_2, and i_3 as the currents through resistors R_1, R_2, and R_3, respectively. At node 1, applying KCL gives

$$I_1 = I_2 + i_1 + i_2 \tag{3.1}$$

At node 2,

$$I_2 + i_2 = i_3 \tag{3.2}$$

We now apply Ohm's law to express the unknown currents i_1, i_2, and i_3 in terms of node voltages. The key idea to bear in mind is that, since resistance is a passive element, by the passive sign convention, current must always flow from a higher potential to a lower potential.

Current flows from **a higher** potential to **a lower** potential in a resistor.

We can express this principle as

$$i = \frac{v_{higher} - v_{lower}}{R} \tag{3.3}$$

Note that this principle is in agreement with the way we defined resistance in Chapter 2 (see Fig. 2.1). With this in mind, we obtain from Fig. 3.2(b),

$$i_1 = \frac{v_1 - 0}{R_1} \quad \text{or} \quad i_1 = G_1 v_1$$
$$i_2 = \frac{v_1 - v_2}{R_2} \quad \text{or} \quad i_2 = G_2(v_1 - v_2) \tag{3.4}$$
$$i_3 = \frac{v_2 - 0}{R_3} \quad \text{or} \quad i_3 = G_3 v_2$$

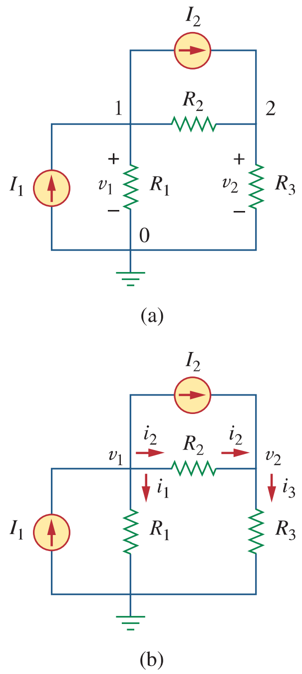


Figure 3.2
Typical circuit for nodal analysis.

Substituting Eq. (3.4) in Eqs. (3.1) and (3.2) results, respectively, in

$$I_1 = I_2 + \frac{v_1}{R_1} + \frac{v_1 - v_2}{R_2} \tag{3.5}$$

$$I_2 + \frac{v_1 - v_2}{R_2} = \frac{v_2}{R_3} \tag{3.6}$$

In terms of the conductances, Eqs. (3.5) and (3.6) become

$$I_1 = I_2 + G_1 v_1 + G_2(v_1 - v_2) \tag{3.7}$$

$$I_2 + G_2(v_1 - v_2) = G_3 v_2 \tag{3.8}$$

The third step in nodal analysis is to solve for the node voltages. If we apply KCL to $n - 1$ nonreference nodes, we obtain $n - 1$ simultaneous equations such as Eqs. (3.5) and (3.6) or (3.7) and (3.8). For the circuit of Fig. 3.2, we solve Eqs. (3.5) and (3.6) or (3.7) and (3.8) to obtain the node voltages v_1 and v_2 using any standard method, such as the substitution method, the elimination method, Cramer's rule, or matrix inversion. To use either of the last two methods, one must cast the simultaneous equations in matrix form. For example, Eqs. (3.7) and (3.8) can be cast in matrix form as

Appendix A discusses how to use Cramer's rule.

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix} \tag{3.9}$$

which can be solved to get v_1 and v_2. Equation 3.9 will be generalized in Section 3.6. The simultaneous equations may also be solved using calculators or with software packages such as *MATLAB*, *Mathcad*, *Maple*, and *Quattro Pro*.

Example 3.1

Calculate the node voltages in the circuit shown in Fig. 3.3(a).

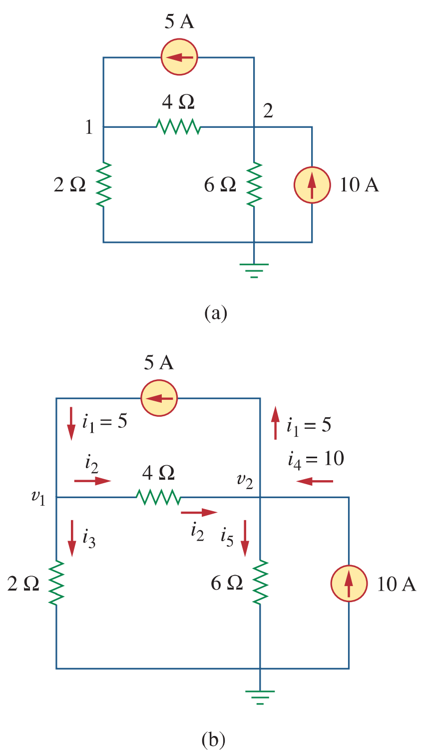


Figure 3.3
For Example 3.1: (a) original circuit, (b) circuit for analysis.

Solution:
Consider Fig. 3.3(b), where the circuit in Fig. 3.3(a) has been prepared for nodal analysis. Notice how the currents are selected for the application of KCL. Except for the branches with current sources, the labeling of the currents is arbitrary but consistent. (By consistent, we mean that if, for example, we assume that i_2 enters the 4-Ω resistor from the left-hand side, i_2 must leave the resistor from the right-hand side.) The reference node is selected, and the node voltages v_1 and v_2 are now to be determined.

At node 1, applying KCL and Ohm's law gives

$$i_1 = i_2 + i_3 \quad \Rightarrow \quad 5 = \frac{v_1 - v_2}{4} + \frac{v_1 - 0}{2}$$

Multiplying each term in the last equation by 4, we obtain

$$20 = v_1 - v_2 + 2v_1$$

or

$$3v_1 - v_2 = 20 \tag{3.1.1}$$

At node 2, we do the same thing and get

$$i_2 + i_4 = i_1 + i_5 \quad \Rightarrow \quad \frac{v_1 - v_2}{4} + 10 = 5 + \frac{v_2 - 0}{6}$$

Multiplying each term by 12 results in

$$3v_1 - 3v_2 + 120 = 60 + 2v_2$$

or

$$-3v_1 + 5v_2 = 60 \tag{3.1.2}$$

Now we have two simultaneous Eqs. (3.1.1) and (3.1.2). We can solve the equations using any method and obtain the values of v_1 and v_2.

METHOD 1 Using the elimination technique, we add Eqs. (3.1.1) and (3.1.2).

$$4v_2 = 80 \quad \Rightarrow \quad v_2 = 20 \text{ V}$$

Substituting $v_2 = 20$ in Eq. (3.1.1) gives

$$3v_1 - 20 = 20 \quad \Rightarrow \quad v_1 = \frac{40}{3} = 13.333 \text{ V}$$

METHOD 2 To use Cramer's rule, we need to put Eqs. (3.1.1) and (3.1.2) in matrix form as

$$\begin{bmatrix} 3 & -1 \\ -3 & 5 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 20 \\ 60 \end{bmatrix} \tag{3.1.3}$$

The determinant of the matrix is

$$\Delta = \begin{vmatrix} 3 & -1 \\ -3 & 5 \end{vmatrix} = 15 - 3 = 12$$

We now obtain v_1 and v_2 as

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{\begin{vmatrix} 20 & -1 \\ 60 & 5 \end{vmatrix}}{\Delta} = \frac{100 + 60}{12} = 13.333 \text{ V}$$

$$v_2 = \frac{\Delta_2}{\Delta} = \frac{\begin{vmatrix} 3 & 20 \\ -3 & 60 \end{vmatrix}}{\Delta} = \frac{180 + 60}{12} = 20 \text{ V}$$

giving us the same result as did the elimination method.

If we need the currents, we can easily calculate them from the values of the nodal voltages.

$$i_1 = 5 \text{ A}, \qquad i_2 = \frac{v_1 - v_2}{4} = -1.6668 \text{ A}, \qquad i_3 = \frac{v_1}{2} = 6.666 \text{ A}$$

$$i_4 = 10 \text{ A}, \qquad i_5 = \frac{v_2}{6} = 3.333 \text{ A}$$

The fact that i_2 is negative shows that the current flows in the direction opposite to the one assumed.

Practice Problem 3.1

Obtain the node voltages in the circuit of Fig. 3.4.

Answer: $v_1 = -6$ V, $v_2 = -42$ V.

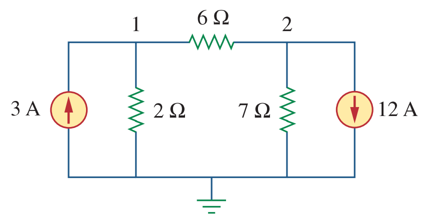


Figure 3.4
For Practice Prob. 3.1.

Example 3.2

Determine the voltages at the nodes in Fig. 3.5(a).

Solution:

The circuit in this example has three nonreference nodes, unlike the previous example which has two nonreference nodes. We assign voltages to the three nodes as shown in Fig. 3.5(b) and label the currents.

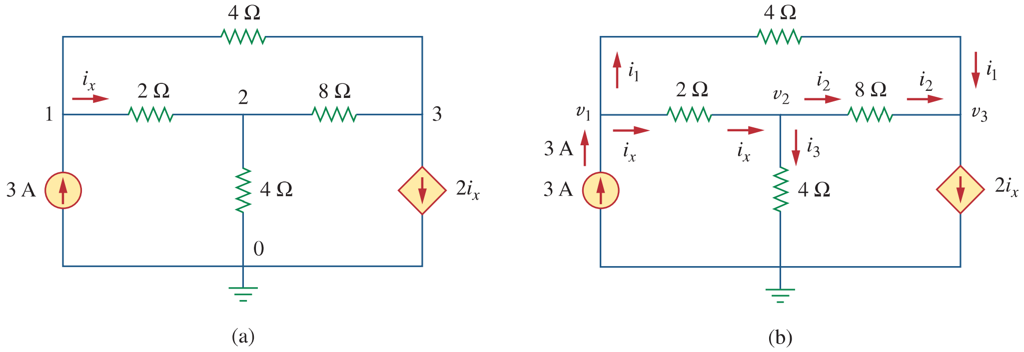


Figure 3.5
For Example 3.2: (a) original circuit, (b) circuit for analysis.

At node 1,

$$3 = i_1 + i_x \quad \Rightarrow \quad 3 = \frac{v_1 - v_3}{4} + \frac{v_1 - v_2}{2}$$

Multiplying by 4 and rearranging terms, we get

$$3v_1 - 2v_2 - v_3 = 12 \tag{3.2.1}$$

At node 2,

$$i_x = i_2 + i_3 \quad \Rightarrow \quad \frac{v_1 - v_2}{2} = \frac{v_2 - v_3}{8} + \frac{v_2 - 0}{4}$$

Multiplying by 8 and rearranging terms, we get

$$-4v_1 + 7v_2 - v_3 = 0 \tag{3.2.2}$$

At node 3,

$$i_1 + i_2 = 2i_x \quad \Rightarrow \quad \frac{v_1 - v_3}{4} + \frac{v_2 - v_3}{8} = \frac{2(v_1 - v_2)}{2}$$

Multiplying by 8, rearranging terms, and dividing by 3, we get

$$2v_1 - 3v_2 + v_3 = 0 \tag{3.2.3}$$

We have three simultaneous equations to solve to get the node voltages v_1, v_2, and v_3. We shall solve the equations in three ways.

■ **METHOD 1** Using the elimination technique, we add Eqs. (3.2.1) and (3.2.3).

$$5v_1 - 5v_2 = 12$$

or

$$v_1 - v_2 = \frac{12}{5} = 2.4 \tag{3.2.4}$$

Adding Eqs. (3.2.2) and (3.2.3) gives

$$-2v_1 + 4v_2 = 0 \quad \Rightarrow \quad v_1 = 2v_2 \tag{3.2.5}$$

Substituting Eq. (3.2.5) into Eq. (3.2.4) yields

$$2v_2 - v_2 = 2.4 \quad \Rightarrow \quad v_2 = 2.4, \quad v_1 = 2v_2 = 4.8 \text{ V}$$

From Eq. (3.2.3), we get

$$v_3 = 3v_2 - 2v_1 = 3v_2 - 4v_2 = -v_2 = -2.4 \text{ V}$$

Thus,

$$v_1 = 4.8 \text{ V}, \quad v_2 = 2.4 \text{ V}, \quad v_3 = -2.4 \text{ V}$$

METHOD 2 To use Cramer's rule, we put Eqs. (3.2.1) to (3.2.3) in matrix form.

$$\begin{bmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix} \tag{3.2.6}$$

From this, we obtain

$$v_1 = \frac{\Delta_1}{\Delta}, \quad v_2 = \frac{\Delta_2}{\Delta}, \quad v_3 = \frac{\Delta_3}{\Delta}$$

where Δ, Δ_1, Δ_2, and Δ_3 are the determinants to be calculated as follows. As explained in Appendix A, to calculate the determinant of a 3 by 3 matrix, we repeat the first two rows and cross multiply.

$$\Delta = \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \end{vmatrix} = \begin{vmatrix} 3 & -2 & -1 \\ -4 & 7 & -1 \\ 2 & -3 & 1 \\ 3 & -2 & -1 \\ -4 & 7 & -1 \end{vmatrix}$$

$$= 21 - 12 + 4 + 14 - 9 - 8 = 10$$

Similarly, we obtain

$$\Delta_1 = \begin{vmatrix} 12 & -2 & -1 \\ 0 & 7 & -1 \\ 0 & -3 & 1 \\ 12 & -2 & -1 \\ 0 & 7 & -1 \end{vmatrix} = 84 + 0 + 0 - 0 - 36 - 0 = 48$$

$$\Delta_2 = \begin{vmatrix} 3 & 12 & -1 \\ -4 & 0 & -1 \\ 2 & 0 & 1 \\ 3 & 12 & -1 \\ -4 & 0 & -1 \end{vmatrix} = 0 + 0 - 24 - 0 - 0 + 48 = 24$$

$$\Delta_3 = \begin{vmatrix} 3 & -2 & 12 \\ -4 & 7 & 0 \\ 2 & -3 & 0 \\ 3 & -2 & 12 \\ -4 & 7 & 0 \end{vmatrix} = 0 + 144 + 0 - 168 - 0 - 0 = -24$$

Thus, we find

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{48}{10} = 4.8 \text{ V}, \qquad v_2 = \frac{\Delta_2}{\Delta} = \frac{24}{10} = 2.4 \text{ V}$$

$$v_3 = \frac{\Delta_3}{\Delta} = \frac{-24}{10} = -2.4 \text{ V}$$

as we obtained with Method 1.

■ **METHOD 3** We now use *MATLAB* to solve the matrix. Equation (3.2.6) can be written as

$$\mathbf{AV} = \mathbf{B} \quad \Rightarrow \quad \mathbf{V} = \mathbf{A}^{-1}\mathbf{B}$$

where **A** is the 3 by 3 square matrix, **B** is the column vector, and **V** is a column vector comprised of v_1, v_2, and v_3 that we want to determine. We use *MATLAB* to determine **V** as follows:

```
>>A = [3  -2  -1;  -4  7  -1;  2  -3  1];
>>B = [12  0  0]';
>>V = inv(A) * B
        4.8000
   V =  2.4000
       -2.4000
```

Thus, $v_1 = 4.8$ V, $v_2 = 2.4$ V, and $v_3 = -2.4$ V, as obtained previously.

Practice Problem 3.2

Find the voltages at the three nonreference nodes in the circuit of Fig. 3.6.

Answer: $v_1 = 32$ V, $v_2 = -25.6$ V, $v_3 = 62.4$ V.

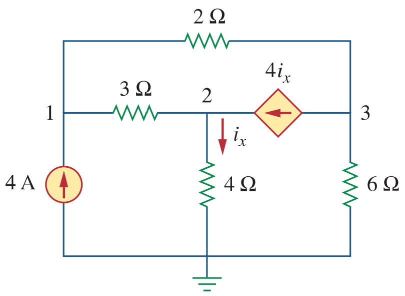


Figure 3.6
For Practice Prob. 3.2.

3.3 Nodal Analysis with Voltage Sources

We now consider how voltage sources affect nodal analysis. We use the circuit in Fig. 3.7 for illustration. Consider the following two possibilities.

■ **CASE 1** If a voltage source is connected between the reference node and a nonreference node, we simply set the voltage at the nonreference node equal to the voltage of the voltage source. In Fig. 3.7, for example,

$$v_1 = 10 \text{ V} \tag{3.10}$$

Thus, our analysis is somewhat simplified by this knowledge of the voltage at this node.

■ **CASE 2** If the voltage source (dependent or independent) is connected between two nonreference nodes, the two nonreference nodes

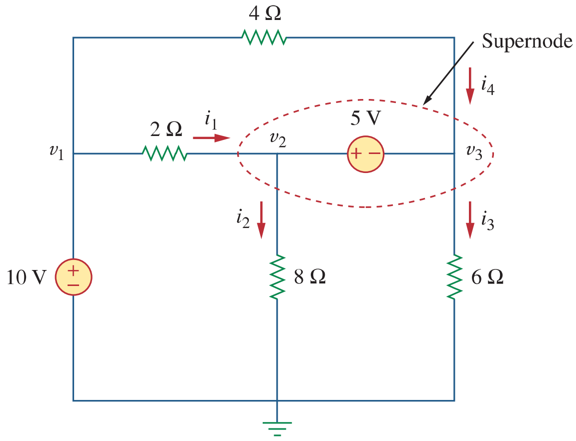


Figure 3.7
A circuit with a supernode.

form a *generalized node* or *supernode*; we apply both KCL and KVL to determine the node voltages.

A supernode may be regarded as a closed surface enclosing the voltage source and its two nodes.

> A **supernode** is formed by enclosing a (dependent or independent) voltage source connected between two nonreference nodes and any elements connected in parallel with it.

In Fig. 3.7, nodes 2 and 3 form a supernode. (We could have more than two nodes forming a single supernode. For example, see the circuit in Fig. 3.14.) We analyze a circuit with supernodes using the same three steps mentioned in the previous section except that the supernodes are treated differently. Why? Because an essential component of nodal analysis is applying KCL, which requires knowing the current through each element. There is no way of knowing the current through a voltage source in advance. However, KCL must be satisfied at a supernode like any other node. Hence, at the supernode in Fig. 3.7,

$$i_1 + i_4 = i_2 + i_3 \tag{3.11a}$$

or

$$\frac{v_1 - v_2}{2} + \frac{v_1 - v_3}{4} = \frac{v_2 - 0}{8} + \frac{v_3 - 0}{6} \tag{3.11b}$$

To apply Kirchhoff's voltage law to the supernode in Fig. 3.7, we redraw the circuit as shown in Fig. 3.8. Going around the loop in the clockwise direction gives

$$-v_2 + 5 + v_3 = 0 \quad \Rightarrow \quad v_2 - v_3 = 5 \tag{3.12}$$

From Eqs. (3.10), (3.11b), and (3.12), we obtain the node voltages.

Note the following properties of a supernode:

1. The voltage source inside the supernode provides a constraint equation needed to solve for the node voltages.
2. A supernode has no voltage of its own.
3. A supernode requires the application of both KCL and KVL.

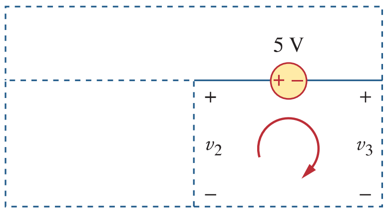


Figure 3.8
Applying KVL to a supernode.

Example 3.3

For the circuit shown in Fig. 3.9, find the node voltages.

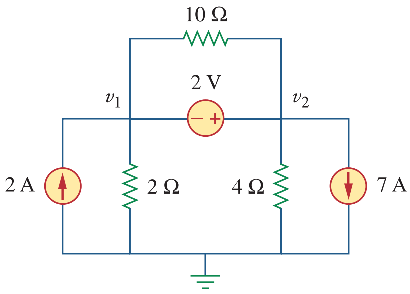


Figure 3.9
For Example 3.3.

Solution:
The supernode contains the 2-V source, nodes 1 and 2, and the 10-Ω resistor. Applying KCL to the supernode as shown in Fig. 3.10(a) gives

$$2 = i_1 + i_2 + 7$$

Expressing i_1 and i_2 in terms of the node voltages

$$2 = \frac{v_1 - 0}{2} + \frac{v_2 - 0}{4} + 7 \quad \Rightarrow \quad 8 = 2v_1 + v_2 + 28$$

or

$$v_2 = -20 - 2v_1 \tag{3.3.1}$$

To get the relationship between v_1 and v_2, we apply KVL to the circuit in Fig. 3.10(b). Going around the loop, we obtain

$$-v_1 - 2 + v_2 = 0 \quad \Rightarrow \quad v_2 = v_1 + 2 \tag{3.3.2}$$

From Eqs. (3.3.1) and (3.3.2), we write

$$v_2 = v_1 + 2 = -20 - 2v_1$$

or

$$3v_1 = -22 \quad \Rightarrow \quad v_1 = -7.333 \text{ V}$$

and $v_2 = v_1 + 2 = -5.333$ V. Note that the 10-Ω resistor does not make any difference because it is connected across the supernode.

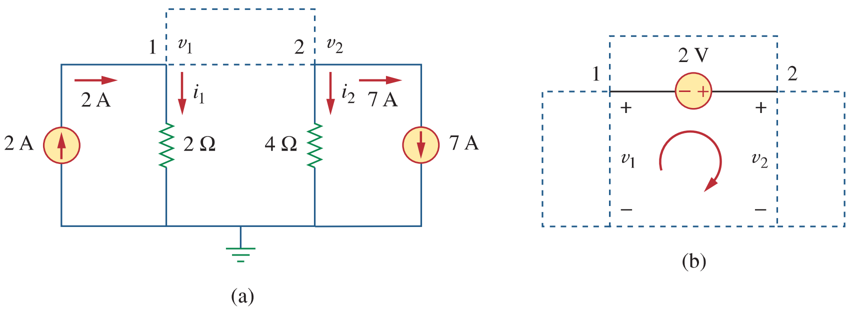


Figure 3.10
Applying: (a) KCL to the supernode, (b) KVL to the loop.

Practice Problem 3.3

Find v and i in the circuit of Fig. 3.11.

Answer: −400 mV, 2.8 A.

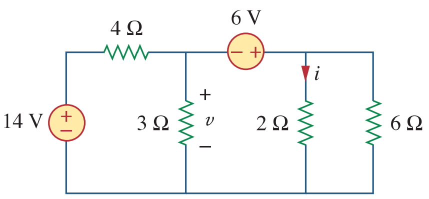


Figure 3.11
For Practice Prob. 3.3.

Find the node voltages in the circuit of Fig. 3.12.

Example 3.4

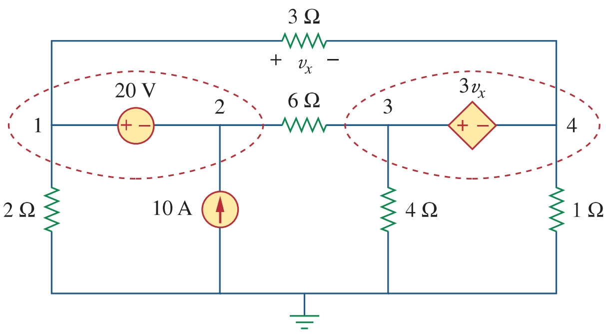


Figure 3.12
For Example 3.4.

Solution:
Nodes 1 and 2 form a supernode; so do nodes 3 and 4. We apply KCL to the two supernodes as in Fig. 3.13(a). At supernode 1-2,

$$i_3 + 10 = i_1 + i_2$$

Expressing this in terms of the node voltages,

$$\frac{v_3 - v_2}{6} + 10 = \frac{v_1 - v_4}{3} + \frac{v_1}{2}$$

or

$$5v_1 + v_2 - v_3 - 2v_4 = 60 \qquad \textbf{(3.4.1)}$$

At supernode 3-4,

$$i_1 = i_3 + i_4 + i_5 \qquad \Rightarrow \qquad \frac{v_1 - v_4}{3} = \frac{v_3 - v_2}{6} + \frac{v_4}{1} + \frac{v_3}{4}$$

or

$$4v_1 + 2v_2 - 5v_3 - 16v_4 = 0 \qquad \textbf{(3.4.2)}$$

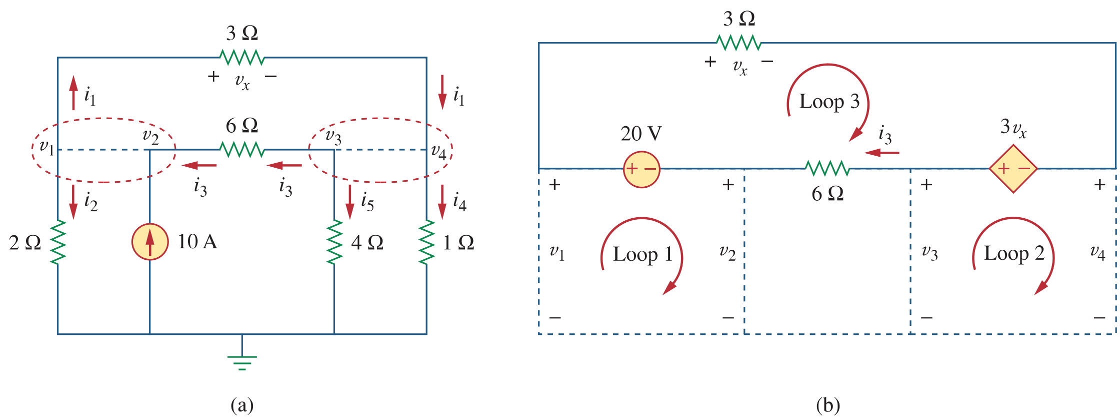


Figure 3.13
Applying: (a) KCL to the two supernodes, (b) KVL to the loops.

We now apply KVL to the branches involving the voltage sources as shown in Fig. 3.13(b). For loop 1,

$$-v_1 + 20 + v_2 = 0 \quad \Rightarrow \quad v_1 - v_2 = 20 \qquad \textbf{(3.4.3)}$$

For loop 2,

$$-v_3 + 3v_x + v_4 = 0$$

But $v_x = v_1 - v_4$ so that

$$3v_1 - v_3 - 2v_4 = 0 \qquad \textbf{(3.4.4)}$$

For loop 3,

$$v_x - 3v_x + 6i_3 - 20 = 0$$

But $6i_3 = v_3 - v_2$ and $v_x = v_1 - v_4$. Hence,

$$-2v_1 - v_2 + v_3 + 2v_4 = 20 \qquad \textbf{(3.4.5)}$$

We need four node voltages, v_1, v_2, v_3, and v_4, and it requires only four out of the five Eqs. (3.4.1) to (3.4.5) to find them. Although the fifth equation is redundant, it can be used to check results. We can solve Eqs. (3.4.1) to (3.4.4) directly using *MATLAB*. We can eliminate one node voltage so that we solve three simultaneous equations instead of four. From Eq. (3.4.3), $v_2 = v_1 - 20$. Substituting this into Eqs. (3.4.1) and (3.4.2), respectively, gives

$$6v_1 - v_3 - 2v_4 = 80 \qquad \textbf{(3.4.6)}$$

and

$$6v_1 - 5v_3 - 16v_4 = 40 \qquad \textbf{(3.4.7)}$$

Equations (3.4.4), (3.4.6), and (3.4.7) can be cast in matrix form as

$$\begin{bmatrix} 3 & -1 & -2 \\ 6 & -1 & -2 \\ 6 & -5 & -16 \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 80 \\ 40 \end{bmatrix}$$

Using Cramer's rule gives

$$\Delta = \begin{vmatrix} 3 & -1 & -2 \\ 6 & -1 & -2 \\ 6 & -5 & -16 \end{vmatrix} = -18, \qquad \Delta_1 = \begin{vmatrix} 0 & -1 & -2 \\ 80 & -1 & -2 \\ 40 & -5 & -16 \end{vmatrix} = -480,$$

$$\Delta_3 = \begin{vmatrix} 3 & 0 & -2 \\ 6 & 80 & -2 \\ 6 & 40 & -16 \end{vmatrix} = -3120, \qquad \Delta_4 = \begin{vmatrix} 3 & -1 & 0 \\ 6 & -1 & 80 \\ 6 & -5 & 40 \end{vmatrix} = 840$$

Thus, we arrive at the node voltages as

$$v_1 = \frac{\Delta_1}{\Delta} = \frac{-480}{-18} = 26.67 \text{ V}, \qquad v_3 = \frac{\Delta_3}{\Delta} = \frac{-3120}{-18} = 173.33 \text{ V},$$

$$v_4 = \frac{\Delta_4}{\Delta} = \frac{840}{-18} = -46.67 \text{ V}$$

and $v_2 = v_1 - 20 = 6.667$ V. We have not used Eq. (3.4.5); it can be used to cross check results.

Practice Problem 3.4

Find v_1, v_2, and v_3 in the circuit of Fig. 3.14 using nodal analysis.

Answer: $v_1 = 7.608$ V, $v_2 = -17.39$ V, $v_3 = 1.6305$ V.

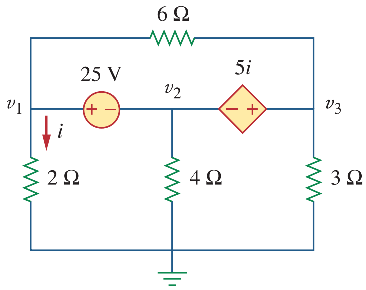


Figure 3.14
For Practice Prob. 3.4.

3.4 Mesh Analysis

Mesh analysis provides another general procedure for analyzing circuits, using mesh currents as the circuit variables. Using mesh currents instead of element currents as circuit variables is convenient and reduces the number of equations that must be solved simultaneously. Recall that a loop is a closed path with no node passed more than once. A mesh is a loop that does not contain any other loop within it.

Mesh analysis is also known as *loop analysis* or the *mesh-current method*.

Nodal analysis applies KCL to find unknown voltages in a given circuit, while mesh analysis applies KVL to find unknown currents. Mesh analysis is not quite as general as nodal analysis because it is only applicable to a circuit that is *planar*. A planar circuit is one that can be drawn in a plane with no branches crossing one another; otherwise it is *nonplanar*. A circuit may have crossing branches and still be planar if it can be redrawn such that it has no crossing branches. For example, the circuit in Fig. 3.15(a) has two crossing branches, but it can be redrawn as in Fig. 3.15(b). Hence, the circuit in Fig. 3.15(a) is planar. However, the circuit in Fig. 3.16 is nonplanar, because there is no way to redraw it and avoid the branches crossing. Nonplanar circuits can be handled using nodal analysis, but they will not be considered in this text.

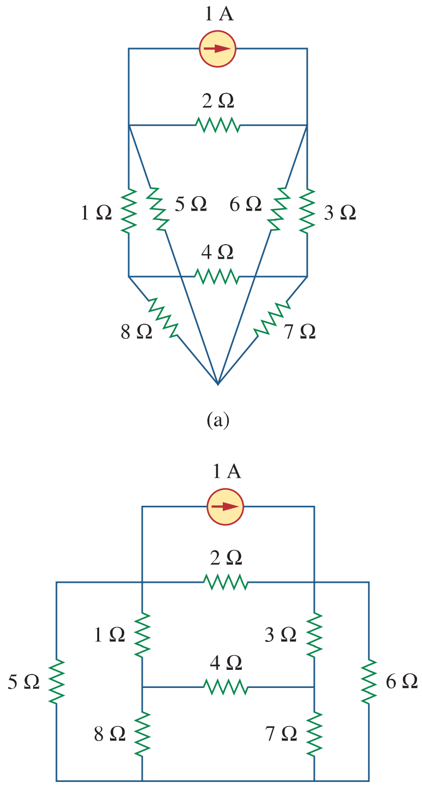


Figure 3.15
(a) A planar circuit with crossing branches, (b) the same circuit redrawn with no crossing branches.

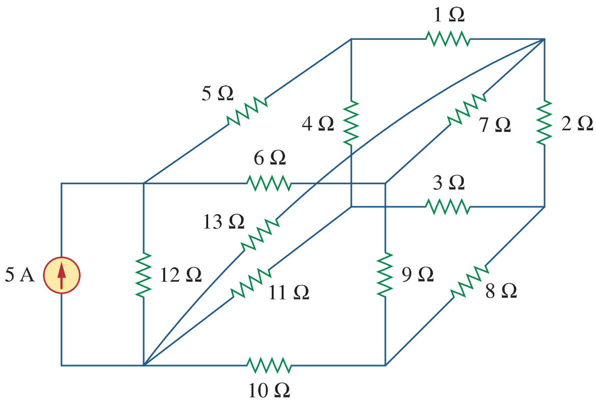


Figure 3.16
A nonplanar circuit.

To understand mesh analysis, we should first explain more about what we mean by a mesh.

A **mesh** is a loop which does not contain any other loops within it.

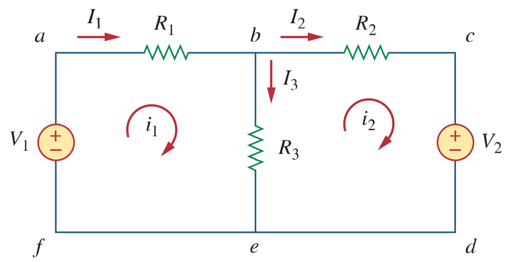


Figure 3.17
A circuit with two meshes.

In Fig. 3.17, for example, paths *abefa* and *bcdeb* are meshes, but path *abcdefa* is not a mesh. The current through a mesh is known as *mesh current.* In mesh analysis, we are interested in applying KVL to find the mesh currents in a given circuit.

Although path *abcdefa* is a loop and not a mesh, KVL still holds. This is the reason for loosely using the terms *loop analysis* and *mesh analysis* to mean the same thing.

In this section, we will apply mesh analysis to planar circuits that do not contain current sources. In the next section, we will consider circuits with current sources. In the mesh analysis of a circuit with n meshes, we take the following three steps.

Steps to Determine Mesh Currents:

1. Assign mesh currents $i_1, i_2, \ldots, i_n$ to the n meshes.
2. Apply KVL to each of the n meshes. Use Ohm's law to express the voltages in terms of the mesh currents.
3. Solve the resulting n simultaneous equations to get the mesh currents.

The direction of the mesh current is arbitrary—(clockwise or counterclockwise)—and does not affect the validity of the solution.

To illustrate the steps, consider the circuit in Fig. 3.17. The first step requires that mesh currents i_1 and i_2 are assigned to meshes 1 and 2. Although a mesh current may be assigned to each mesh in an arbitrary direction, it is conventional to assume that each mesh current flows clockwise.

As the second step, we apply KVL to each mesh. Applying KVL to mesh 1, we obtain

$$-V_1 + R_1 i_1 + R_3(i_1 - i_2) = 0$$

or

$$(R_1 + R_3)i_1 - R_3 i_2 = V_1 \tag{3.13}$$

For mesh 2, applying KVL gives

$$R_2 i_2 + V_2 + R_3(i_2 - i_1) = 0$$

or

$$-R_3 i_1 + (R_2 + R_3)i_2 = -V_2 \tag{3.14}$$

Note in Eq. (3.13) that the coefficient of i_1 is the sum of the resistances in the first mesh, while the coefficient of i_2 is the negative of the resistance common to meshes 1 and 2. Now observe that the same is true in Eq. (3.14). This can serve as a shortcut way of writing the mesh equations. We will exploit this idea in Section 3.6.

The shortcut way will not apply if one mesh current is assumed clockwise and the other assumed counterclockwise, although this is permissible.

The third step is to solve for the mesh currents. Putting Eqs. (3.13) and (3.14) in matrix form yields

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} V_1 \\ -V_2 \end{bmatrix} \tag{3.15}$$

which can be solved to obtain the mesh currents i_1 and i_2. We are at liberty to use any technique for solving the simultaneous equations. According to Eq. (2.12), if a circuit has n nodes, b branches, and l independent loops or meshes, then $l = b - n + 1$. Hence, l independent simultaneous equations are required to solve the circuit using mesh analysis.

Notice that the branch currents are different from the mesh currents unless the mesh is isolated. To distinguish between the two types of currents, we use i for a mesh current and I for a branch current. The current elements I_1, I_2, and I_3 are algebraic sums of the mesh currents. It is evident from Fig. 3.17 that

$$I_1 = i_1, \qquad I_2 = i_2, \qquad I_3 = i_1 - i_2 \tag{3.16}$$

Example 3.5

For the circuit in Fig. 3.18, find the branch currents I_1, I_2, and I_3 using mesh analysis.

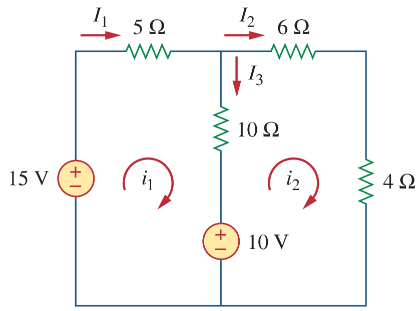


Figure 3.18
For Example 3.5.

Solution:
We first obtain the mesh currents using KVL. For mesh 1,

$$-15 + 5i_1 + 10(i_1 - i_2) + 10 = 0$$

or

$$3i_1 - 2i_2 = 1 \tag{3.5.1}$$

For mesh 2,

$$6i_2 + 4i_2 + 10(i_2 - i_1) - 10 = 0$$

or

$$i_1 = 2i_2 - 1 \tag{3.5.2}$$

■ **METHOD 1** Using the substitution method, we substitute Eq. (3.5.2) into Eq. (3.5.1), and write

$$6i_2 - 3 - 2i_2 = 1 \quad \Rightarrow \quad i_2 = 1 \text{ A}$$

From Eq. (3.5.2), $i_1 = 2i_2 - 1 = 2 - 1 = 1$ A. Thus,

$$I_1 = i_1 = 1 \text{ A}, \qquad I_2 = i_2 = 1 \text{ A}, \qquad I_3 = i_1 - i_2 = 0$$

■ **METHOD 2** To use Cramer's rule, we cast Eqs. (3.5.1) and (3.5.2) in matrix form as

$$\begin{bmatrix} 3 & -2 \\ -1 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} 1 \\ 1 \end{bmatrix}$$

We obtain the determinants

$$\Delta = \begin{vmatrix} 3 & -2 \\ -1 & 2 \end{vmatrix} = 6 - 2 = 4$$

$$\Delta_1 = \begin{vmatrix} 1 & -2 \\ 1 & 2 \end{vmatrix} = 2 + 2 = 4, \qquad \Delta_2 = \begin{vmatrix} 3 & 1 \\ -1 & 1 \end{vmatrix} = 3 + 1 = 4$$

Thus,

$$i_1 = \frac{\Delta_1}{\Delta} = 1 \text{ A}, \qquad i_2 = \frac{\Delta_2}{\Delta} = 1 \text{ A}$$

as before.

Practice Problem 3.5

Calculate the mesh currents i_1 and i_2 of the circuit of Fig. 3.19.

Answer: $i_1 = 2.5$ A, $i_2 = 0$ A.

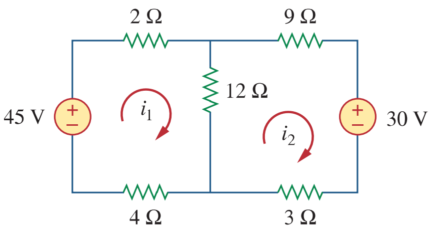


Figure 3.19
For Practice Prob. 3.5.

Example 3.6

Use mesh analysis to find the current I_o in the circuit of Fig. 3.20.

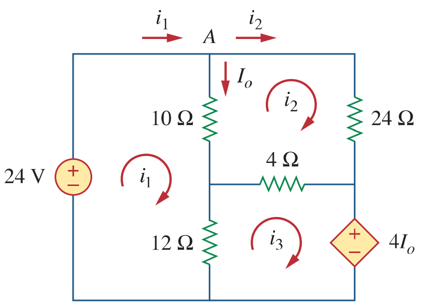


Figure 3.20
For Example 3.6.

Solution:
We apply KVL to the three meshes in turn. For mesh 1,

$$-24 + 10(i_1 - i_2) + 12(i_1 - i_3) = 0$$

or

$$11i_1 - 5i_2 - 6i_3 = 12 \tag{3.6.1}$$

For mesh 2,

$$24i_2 + 4(i_2 - i_3) + 10(i_2 - i_1) = 0$$

or

$$-5i_1 + 19i_2 - 2i_3 = 0 \tag{3.6.2}$$

For mesh 3,

$$4I_o + 12(i_3 - i_1) + 4(i_3 - i_2) = 0$$

But at node A, $I_o = i_1 - i_2$, so that

$$4(i_1 - i_2) + 12(i_3 - i_1) + 4(i_3 - i_2) = 0$$

or

$$-i_1 - i_2 + 2i_3 = 0 \qquad \textbf{(3.6.3)}$$

In matrix form, Eqs. (3.6.1) to (3.6.3) become

$$\begin{bmatrix} 11 & -5 & -6 \\ -5 & 19 & -2 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 12 \\ 0 \\ 0 \end{bmatrix}$$

We obtain the determinants as

$$\Delta = \begin{array}{c|ccc|c} & 11 & -5 & -6 & \\ & -5 & 19 & -2 & \\ & -1 & -1 & 2 & \\ - & 11 & -5 & -6 & + \\ - & -5 & 19 & -2 & + \\ - & & & & + \end{array}$$

$$= 418 - 30 - 10 - 114 - 22 - 50 = 192$$

$$\Delta_1 = \begin{array}{c|ccc|c} & 12 & -5 & -6 & \\ & 0 & 19 & -2 & \\ & 0 & -1 & 2 & \\ - & 12 & -5 & -6 & + \\ - & 0 & 19 & -2 & + \\ - & & & & + \end{array} = 456 - 24 = 432$$

$$\Delta_2 = \begin{array}{c|ccc|c} & 11 & 12 & -6 & \\ & -5 & 0 & -2 & \\ & -1 & 0 & 2 & \\ - & 11 & 12 & -6 & + \\ - & -5 & 0 & -2 & + \\ - & & & & + \end{array} = 24 + 120 = 144$$

$$\Delta_3 = \begin{array}{c|ccc|c} & 11 & -5 & 12 & \\ & -5 & 19 & 0 & \\ & -1 & -1 & 0 & \\ - & 11 & -5 & 12 & + \\ - & -5 & 19 & 0 & + \\ - & & & & + \end{array} = 60 + 228 = 288$$

We calculate the mesh currents using Cramer's rule as

$$i_1 = \frac{\Delta_1}{\Delta} = \frac{432}{192} = 2.25 \text{ A}, \qquad i_2 = \frac{\Delta_2}{\Delta} = \frac{144}{192} = 0.75 \text{ A},$$

$$i_3 = \frac{\Delta_3}{\Delta} = \frac{288}{192} = 1.5 \text{ A}$$

Thus, $I_o = i_1 - i_2 = 1.5$ A.

Practice Problem 3.6

Using mesh analysis, find I_o in the circuit of Fig. 3.21.

Answer: -4 A.

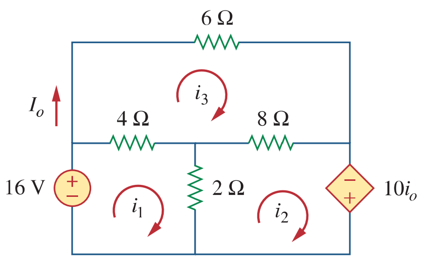


Figure 3.21
For Practice Prob. 3.6.

3.5 Mesh Analysis with Current Sources

Applying mesh analysis to circuits containing current sources (dependent or independent) may appear complicated. But it is actually much easier than what we encountered in the previous section, because the presence of the current sources reduces the number of equations. Consider the following two possible cases.

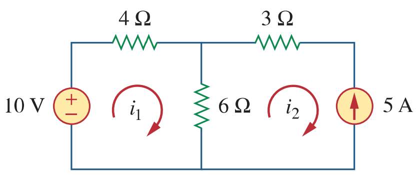


Figure 3.22
A circuit with a current source.

■ **CASE 1** When a current source exists only in one mesh: Consider the circuit in Fig. 3.22, for example. We set $i_2 = -5$ A and write a mesh equation for the other mesh in the usual way; that is,

$$-10 + 4i_1 + 6(i_1 - i_2) = 0 \quad \Rightarrow \quad i_1 = -2 \text{ A} \tag{3.17}$$

■ **CASE 2** When a current source exists between two meshes: Consider the circuit in Fig. 3.23(a), for example. We create a *supermesh* by excluding the current source and any elements connected in series with it, as shown in Fig. 3.23(b). Thus,

> A **supermesh** results when two meshes have a (dependent or independent) current source in common.

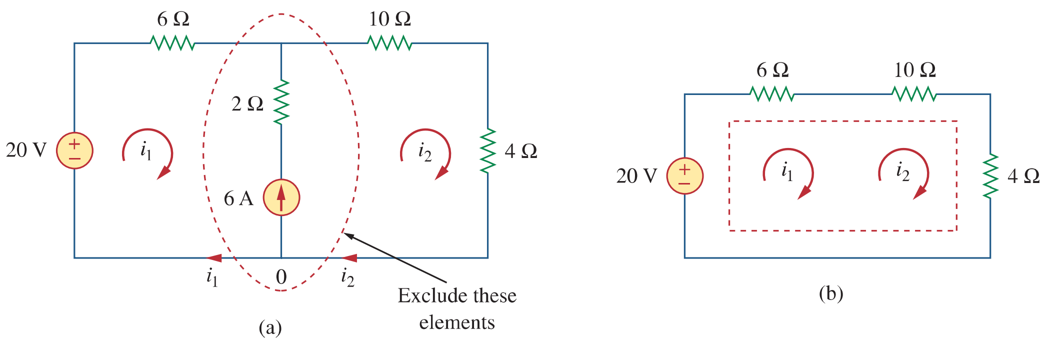


Figure 3.23
(a) Two meshes having a current source in common, (b) a supermesh, created by excluding the current source.

As shown in Fig. 3.23(b), we create a supermesh as the periphery of the two meshes and treat it differently. (If a circuit has two or more supermeshes that intersect, they should be combined to form a larger supermesh.) Why treat the supermesh differently? Because mesh analysis applies KVL—which requires that we know the voltage across each branch—and we do not know the voltage across a current source in advance. However, a supermesh must satisfy KVL like any other mesh. Therefore, applying KVL to the supermesh in Fig. 3.23(b) gives

$$-20 + 6i_1 + 10i_2 + 4i_2 = 0$$

or

$$6i_1 + 14i_2 = 20 \qquad \textbf{(3.18)}$$

We apply KCL to a node in the branch where the two meshes intersect. Applying KCL to node 0 in Fig. 3.23(a) gives

$$i_2 = i_1 + 6 \qquad \textbf{(3.19)}$$

Solving Eqs. (3.18) and (3.19), we get

$$i_1 = -3.2 \text{ A}, \qquad i_2 = 2.8 \text{ A} \qquad \textbf{(3.20)}$$

Note the following properties of a supermesh:

1. The current source in the supermesh provides the constraint equation necessary to solve for the mesh currents.
2. A supermesh has no current of its own.
3. A supermesh requires the application of both KVL and KCL.

Example 3.7

For the circuit in Fig. 3.24, find i_1 to i_4 using mesh analysis.

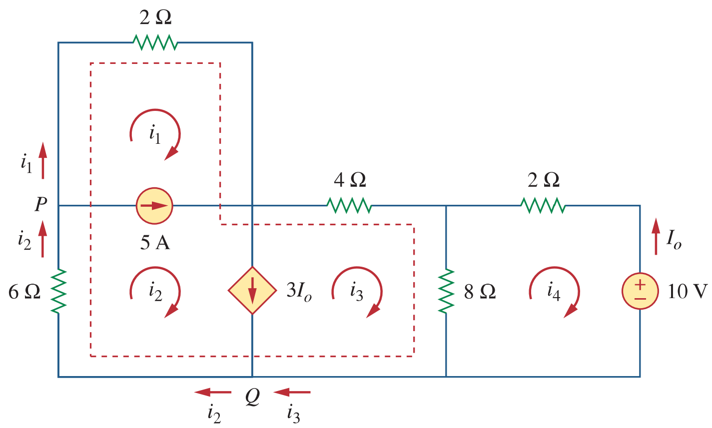


Figure 3.24
For Example 3.7.

Solution:
Note that meshes 1 and 2 form a supermesh since they have an independent current source in common. Also, meshes 2 and 3 form another supermesh because they have a dependent current source in common. The two supermeshes intersect and form a larger supermesh as shown. Applying KVL to the larger supermesh,

$$2i_1 + 4i_3 + 8(i_3 - i_4) + 6i_2 = 0$$

or

$$i_1 + 3i_2 + 6i_3 - 4i_4 = 0 \qquad \textbf{(3.7.1)}$$

For the independent current source, we apply KCL to node P:

$$i_2 = i_1 + 5 \qquad \textbf{(3.7.2)}$$

For the dependent current source, we apply KCL to node Q:

$$i_2 = i_3 + 3I_o$$

But $I_o = -i_4$, hence,

$$i_2 = i_3 - 3i_4 \tag{3.7.3}$$

Applying KVL in mesh 4,

$$2i_4 + 8(i_4 - i_3) + 10 = 0$$

or

$$5i_4 - 4i_3 = -5 \tag{3.7.4}$$

From Eqs. (3.7.1) to (3.7.4),

$$i_1 = -7.5 \text{ A}, \quad i_2 = -2.5 \text{ A}, \quad i_3 = 3.93 \text{ A}, \quad i_4 = 2.143 \text{ A}$$

Practice Problem 3.7

Use mesh analysis to determine i_1, i_2, and i_3 in Fig. 3.25.

Answer: $i_1 = 4.632$ A, $i_2 = 631.6$ mA, $i_3 = 1.4736$ A.

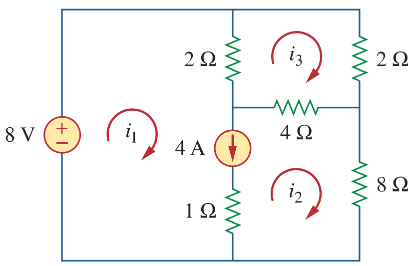


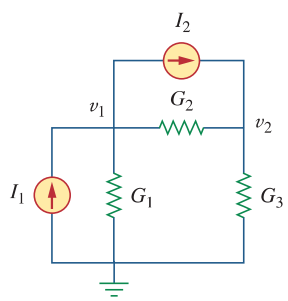
Figure 3.25
For Practice Prob. 3.7.

3.6 †Nodal and Mesh Analyses by Inspection

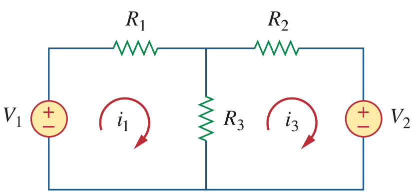
This section presents a generalized procedure for nodal or mesh analysis. It is a shortcut approach based on mere inspection of a circuit.

When all sources in a circuit are independent current sources, we do not need to apply KCL to each node to obtain the node-voltage equations as we did in Section 3.2. We can obtain the equations by mere inspection of the circuit. As an example, let us reexamine the circuit in Fig. 3.2, shown again in Fig. 3.26(a) for convenience. The circuit has two nonreference nodes and the node equations were derived in Section 3.2 as

$$\begin{bmatrix} G_1 + G_2 & -G_2 \\ -G_2 & G_2 + G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} I_1 - I_2 \\ I_2 \end{bmatrix} \tag{3.21}$$



(a)



(b)

Figure 3.26
(a) The circuit in Fig. 3.2, (b) the circuit in Fig. 3.17.

Observe that each of the diagonal terms is the sum of the conductances connected directly to node 1 or 2, while the off-diagonal terms are the negatives of the conductances connected between the nodes. Also, each term on the right-hand side of Eq. (3.21) is the algebraic sum of the currents entering the node.

In general, if a circuit with independent current sources has N nonreference nodes, the node-voltage equations can be written in terms of the conductances as

$$\begin{bmatrix} G_{11} & G_{12} & \dots & G_{1N} \\ G_{21} & G_{22} & \dots & G_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ G_{N1} & G_{N2} & \dots & G_{NN} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} = \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} \tag{3.22}$$

or simply

$$\mathbf{Gv} = \mathbf{i} \tag{3.23}$$

where

G_{kk} = Sum of the conductances connected to node k

$G_{kj} = G_{jk}$ = Negative of the sum of the conductances directly connecting nodes k and j, $k \neq j$

v_k = Unknown voltage at node k

i_k = Sum of all independent current sources directly connected to node k, with currents entering the node treated as positive

G is called the *conductance matrix*; **v** is the output vector; and **i** is the input vector. Equation (3.22) can be solved to obtain the unknown node voltages. Keep in mind that this is valid for circuits with only independent current sources and linear resistors.

Similarly, we can obtain mesh-current equations by inspection when a linear resistive circuit has only independent voltage sources. Consider the circuit in Fig. 3.17, shown again in Fig. 3.26(b) for convenience. The circuit has two nonreference nodes and the node equations were derived in Section 3.4 as

$$\begin{bmatrix} R_1 + R_3 & -R_3 \\ -R_3 & R_2 + R_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} v_1 \\ -v_2 \end{bmatrix} \tag{3.24}$$

We notice that each of the diagonal terms is the sum of the resistances in the related mesh, while each of the off-diagonal terms is the negative of the resistance common to meshes 1 and 2. Each term on the right-hand side of Eq. (3.24) is the algebraic sum taken clockwise of all independent voltage sources in the related mesh.

In general, if the circuit has N meshes, the mesh-current equations can be expressed in terms of the resistances as

$$\begin{bmatrix} R_{11} & R_{12} & \dots & R_{1N} \\ R_{21} & R_{22} & \dots & R_{2N} \\ \vdots & \vdots & \vdots & \vdots \\ R_{N1} & R_{N2} & \dots & R_{NN} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_N \end{bmatrix} = \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_N \end{bmatrix} \tag{3.25}$$

or simply

$$\mathbf{Ri} = \mathbf{v} \tag{3.26}$$

where

R_{kk} = Sum of the resistances in mesh k

$R_{kj} = R_{jk}$ = Negative of the sum of the resistances in common with meshes k and j, $k \neq j$

i_k = Unknown mesh current for mesh k in the clockwise direction

v_k = Sum taken clockwise of all independent voltage sources in mesh k, with voltage rise treated as positive

R is called the *resistance matrix*; **i** is the output vector; and **v** is the input vector. We can solve Eq. (3.25) to obtain the unknown mesh currents.

Example 3.8

Write the node-voltage matrix equations for the circuit in Fig. 3.27 by inspection.

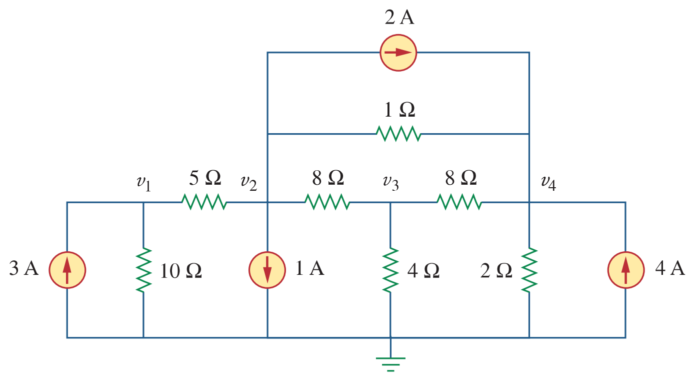


Figure 3.27
For Example 3.8.

Solution:

The circuit in Fig. 3.27 has four nonreference nodes, so we need four node equations. This implies that the size of the conductance matrix **G**, is 4 by 4. The diagonal terms of **G**, in siemens, are

$$G_{11} = \frac{1}{5} + \frac{1}{10} = 0.3, \qquad G_{22} = \frac{1}{5} + \frac{1}{8} + \frac{1}{1} = 1.325$$

$$G_{33} = \frac{1}{8} + \frac{1}{8} + \frac{1}{4} = 0.5, \qquad G_{44} = \frac{1}{8} + \frac{1}{2} + \frac{1}{1} = 1.625$$

The off-diagonal terms are

$$G_{12} = -\frac{1}{5} = -0.2, \qquad G_{13} = G_{14} = 0$$

$$G_{21} = -0.2, \qquad G_{23} = -\frac{1}{8} = -0.125, \qquad G_{24} = -\frac{1}{1} = -1$$

$$G_{31} = 0, \qquad G_{32} = -0.125, \qquad G_{34} = -\frac{1}{8} = -0.125$$

$$G_{41} = 0, \qquad G_{42} = -1, \qquad G_{43} = -0.125$$

The input current vector **i** has the following terms, in amperes:

$$i_1 = 3, \qquad i_2 = -1 - 2 = -3, \qquad i_3 = 0, \qquad i_4 = 2 + 4 = 6$$

Thus the node-voltage equations are

$$\begin{bmatrix} 0.3 & -0.2 & 0 & 0 \\ -0.2 & 1.325 & -0.125 & -1 \\ 0 & -0.125 & 0.5 & -0.125 \\ 0 & -1 & -0.125 & 1.625 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 3 \\ -3 \\ 0 \\ 6 \end{bmatrix}$$

which can be solved using *MATLAB* to obtain the node voltages v_1, v_2, v_3, and v_4.

Practice Problem 3.8

By inspection, obtain the node-voltage equations for the circuit in Fig. 3.28.

Answer:

$$\begin{bmatrix} 1.25 & -0.2 & -1 & 0 \\ -0.2 & 0.2 & 0 & 0 \\ -1 & 0 & 1.25 & -0.25 \\ 0 & 0 & -0.25 & 1.25 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 5 \\ -3 \\ 2 \end{bmatrix}$$

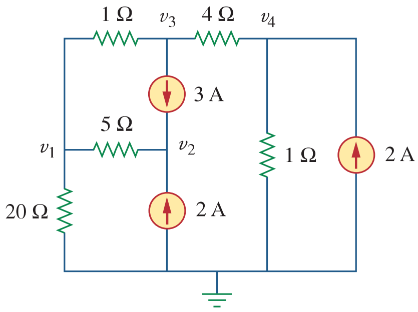


Figure 3.28
For Practice Prob. 3.8.

Example 3.9

By inspection, write the mesh-current equations for the circuit in Fig. 3.29.

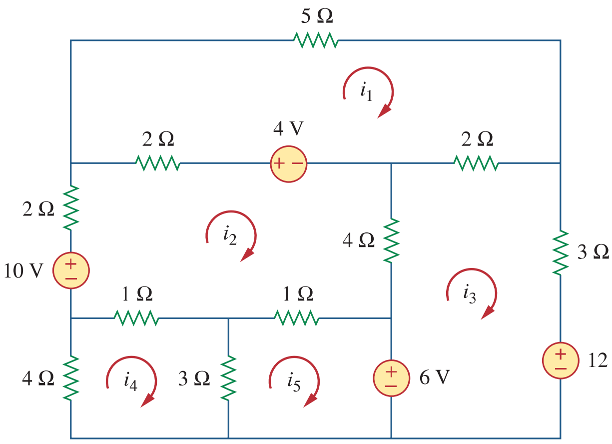


Figure 3.29
For Example 3.9.

Solution:
We have five meshes, so the resistance matrix is 5 by 5. The diagonal terms, in ohms, are:

$$R_{11} = 5 + 2 + 2 = 9, \qquad R_{22} = 2 + 4 + 1 + 1 + 2 = 10,$$
$$R_{33} = 2 + 3 + 4 = 9, \qquad R_{44} = 1 + 3 + 4 = 8, \qquad R_{55} = 1 + 3 = 4$$

The off-diagonal terms are:

$$R_{12} = -2, \qquad R_{13} = -2, \qquad R_{14} = 0 = R_{15},$$
$$R_{21} = -2, \qquad R_{23} = -4, \qquad R_{24} = -1, \qquad R_{25} = -1,$$
$$R_{31} = -2, \qquad R_{32} = -4, \qquad R_{34} = 0 = R_{35},$$
$$R_{41} = 0, \qquad R_{42} = -1, \qquad R_{43} = 0, \qquad R_{45} = -3,$$
$$R_{51} = 0, \qquad R_{52} = -1, \qquad R_{53} = 0, \qquad R_{54} = -3$$

The input voltage vector **v** has the following terms in volts:

$$v_1 = 4, \qquad v_2 = 10 - 4 = 6,$$
$$v_3 = -12 + 6 = -6, \qquad v_4 = 0, \qquad v_5 = -6$$

Thus, the mesh-current equations are:

$$\begin{bmatrix} 9 & -2 & -2 & 0 & 0 \\ -2 & 10 & -4 & -1 & -1 \\ -2 & -4 & 9 & 0 & 0 \\ 0 & -1 & 0 & 8 & -3 \\ 0 & -1 & 0 & -3 & 4 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 4 \\ 6 \\ -6 \\ 0 \\ -6 \end{bmatrix}$$

From this, we can use *MATLAB* to obtain mesh currents i_1, i_2, i_3, i_4, and i_5.

Practice Problem 3.9

By inspection, obtain the mesh-current equations for the circuit in Fig. 3.30.

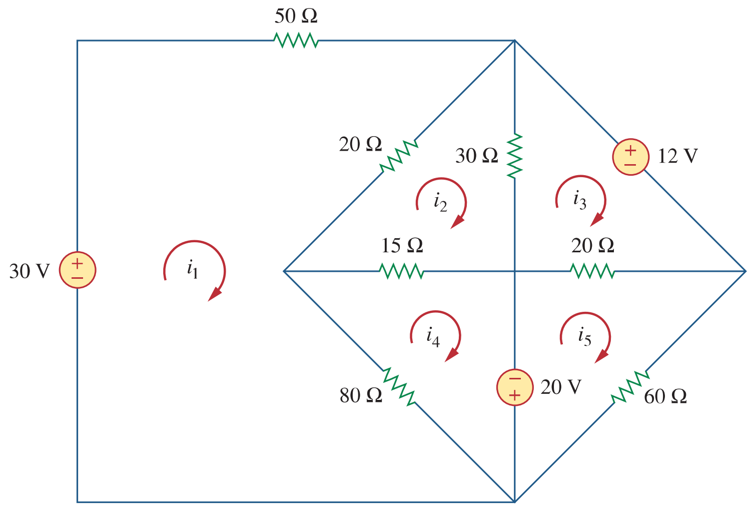


Figure 3.30
For Practice Prob. 3.9.

Answer:

$$\begin{bmatrix} 150 & -40 & 0 & -80 & 0 \\ -40 & 65 & -30 & -15 & 0 \\ 0 & -30 & 50 & 0 & -20 \\ -80 & -15 & 0 & 95 & 0 \\ 0 & 0 & -20 & 0 & 80 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 30 \\ 0 \\ -12 \\ 20 \\ -20 \end{bmatrix}$$

3.7 Nodal Versus Mesh Analysis

Both nodal and mesh analyses provide a systematic way of analyzing a complex network. Someone may ask: Given a network to be analyzed, how do we know which method is better or more efficient? The choice of the better method is dictated by two factors.

The first factor is the nature of the particular network. Networks that contain many series-connected elements, voltage sources, or supermeshes are more suitable for mesh analysis, whereas networks with parallel-connected elements, current sources, or supernodes are more suitable for nodal analysis. Also, a circuit with fewer nodes than meshes is better analyzed using nodal analysis, while a circuit with fewer meshes than nodes is better analyzed using mesh analysis. The key is to select the method that results in the smaller number of equations.

The second factor is the information required. If node voltages are required, it may be expedient to apply nodal analysis. If branch or mesh currents are required, it may be better to use mesh analysis.

It is helpful to be familiar with both methods of analysis, for at least two reasons. First, one method can be used to check the results from the other method, if possible. Second, since each method has its limitations, only one method may be suitable for a particular problem. For example, mesh analysis is the only method to use in analyzing transistor circuits, as we shall see in Section 3.9. But mesh analysis cannot easily be used to solve an op amp circuit, as we shall see in Chapter 5, because there is no direct way to obtain the voltage across the op amp itself. For nonplanar networks, nodal analysis is the only option, because mesh analysis only applies to planar networks. Also, nodal analysis is more amenable to solution by computer, as it is easy to program. This allows one to analyze complicated circuits that defy hand calculation. A computer software package based on nodal analysis is introduced next.

3.8 Circuit Analysis with *PSpice*

PSpice is a computer software circuit analysis program that we will gradually learn to use throughout the course of this text. This section illustrates how to use *PSpice for Windows* to analyze the dc circuits we have studied so far.

Appendix D provides a tutorial on using *PSpice for Windows*.

The reader is expected to review Sections D.1 through D.3 of Appendix D before proceeding in this section. It should be noted that *PSpice* is only helpful in determining branch voltages and currents when the numerical values of all the circuit components are known.

Example 3.10

Use *PSpice* to find the node voltages in the circuit of Fig. 3.31.

Solution:

The first step is to draw the given circuit using Schematics. If one follows the instructions given in Appendix sections D.2 and D.3, the schematic in Fig. 3.32 is produced. Since this is a dc analysis, we use voltage source VDC and current source IDC. The pseudocomponent VIEWPOINTS are added to display the required node voltages. Once the circuit is drawn and saved as *exam310.sch*, we run *PSpice* by selecting **Analysis/Simulate**. The circuit is simulated and the results

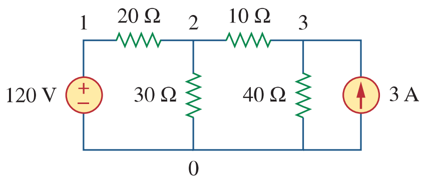


Figure 3.31
For Example 3.10.

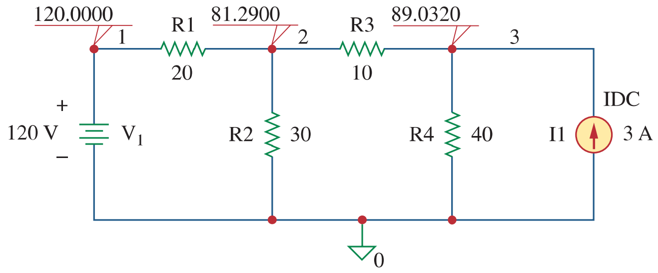


Figure 3.32
For Example 3.10; the schematic of the circuit in Fig. 3.31.

are displayed on VIEWPOINTS and also saved in output file *exam310.out*. The output file includes the following:

```
NODE  VOLTAGE   NODE  VOLTAGE  NODE  VOLTAGE
(1)   120.0000  (2)   81.2900  (3)   89.0320
```

indicating that $V_1 = 120$ V, $V_2 = 81.29$ V, $V_3 = 89.032$ V.

Practice Problem 3.10

For the circuit in Fig. 3.33, use *PSpice* to find the node voltages.

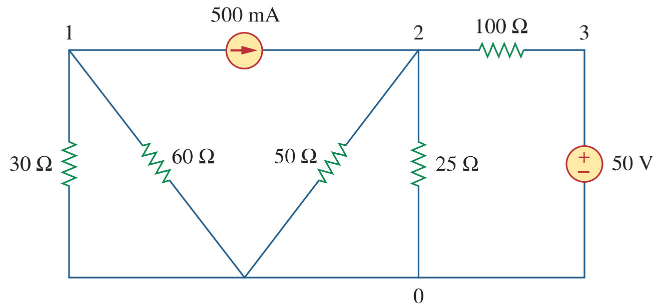


Figure 3.33
For Practice Prob. 3.10.

Answer: $V_1 = -10$ V, $V_2 = 14.286$ V, $V_3 = 50$ V.

Example 3.11

In the circuit of Fig. 3.34, determine the currents i_1, i_2, and i_3.

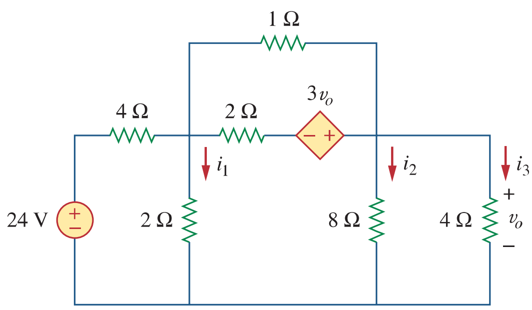


Figure 3.34
For Example 3.11.

Solution:

The schematic is shown in Fig. 3.35. (The schematic in Fig. 3.35 includes the output results, implying that it is the schematic displayed on the screen *after* the simulation.) Notice that the voltage-controlled voltage source E1 in Fig. 3.35 is connected so that its input is the voltage across the 4-Ω resistor; its gain is set equal to 3. In order to display the required currents, we insert pseudocomponent IPROBES in the appropriate branches. The schematic is saved as *exam311.sch* and simulated by selecting **Analysis/Simulate**. The results are displayed on IPROBES as shown in Fig. 3.35 and saved in output file *exam311.out*. From the output file or the IPROBES, we obtain $i_1 = i_2 = 1.333$ A and $i_3 = 2.667$ A.

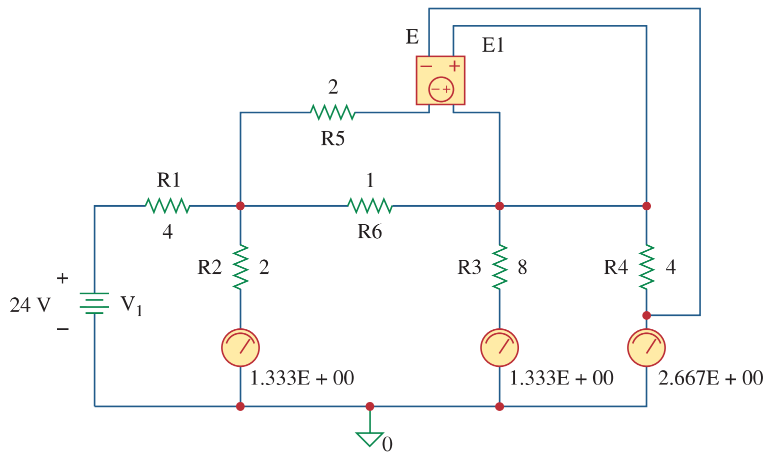


Figure 3.35
The schematic of the circuit in Fig. 3.34.

Practice Problem 3.11

Use *PSpice* to determine currents i_1, i_2, and i_3 in the circuit of Fig. 3.36.

Answer: $i_1 = -428.6$ mA, $i_2 = 2.286$ A, $i_3 = 2$ A.

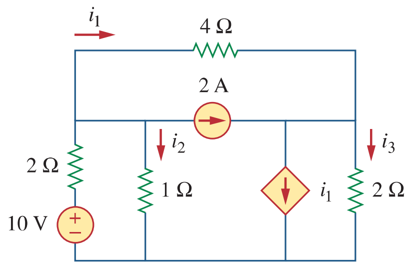


Figure 3.36
For Practice Prob. 3.11.

3.9 †Applications: DC Transistor Circuits

Most of us deal with electronic products on a routine basis and have some experience with personal computers. A basic component for the integrated circuits found in these electronics and computers is the active, three-terminal device known as the *transistor.* Understanding the transistor is essential before an engineer can start an electronic circuit design.

Figure 3.37 depicts various kinds of transistors commercially available. There are two basic types of transistors: *bipolar junction transistors* (BJTs) and *field-effect transistors* (FETs). Here, we consider only the BJTs, which were the first of the two and are still used today. Our objective is to present enough detail about the BJT to enable us to apply the techniques developed in this chapter to analyze dc transistor circuits.

Historical

Courtesy of Lucent Technologies/Bell Labs

William Schockley (1910–1989), **John Bardeen** (1908–1991), and **Walter Brattain** (1902–1987) co-invented the transistor.

Nothing has had a greater impact on the transition from the "Industrial Age" to the "Age of the Engineer" than the transistor. I am sure that Dr. Shockley, Dr. Bardeen, and Dr. Brattain had no idea they would have this incredible effect on our history. While working at Bell Laboratories, they successfully demonstrated the point-contact transistor, invented by Bardeen and Brattain in 1947, and the junction transistor, which Shockley conceived in 1948 and successfully produced in 1951.

It is interesting to note that the idea of the field-effect transistor, the most commonly used one today, was first conceived in 1925–1928 by J. E. Lilienfeld, a German immigrant to the United States. This is evident from his patents of what appears to be a field-effect transistor. Unfortunately, the technology to realize this device had to wait until 1954 when Shockley's field-effect transistor became a reality. Just think what today would be like if we had this transistor 30 years earlier!

For their contributions to the creation of the transistor, Dr. Shockley, Dr. Bardeen, and Dr. Brattain received, in 1956, the Nobel Prize in physics. It should be noted that Dr. Bardeen is the only individual to win two Nobel prizes in physics; the second came later for work in superconductivity at the University of Illinois.

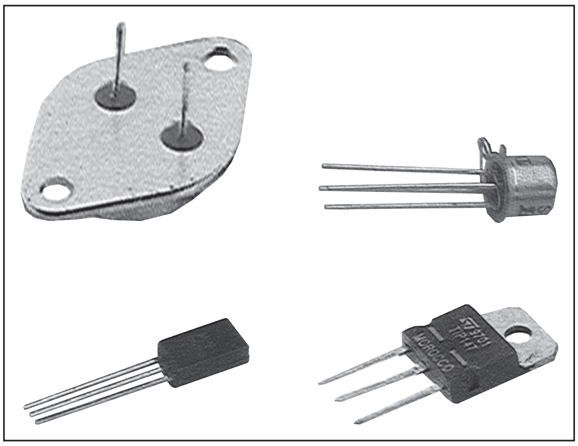


Figure 3.37
Various types of transistors.
(Courtesy of Tech America.)

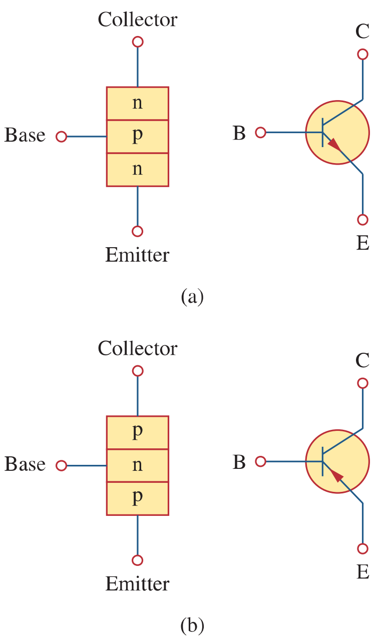


Figure 3.38
Two types of BJTs and their circuit symbols: (a) *npn*, (b) *pnp*.

There are two types of BJTs: *npn* and *pnp*, with their circuit symbols as shown in Fig. 3.38. Each type has three terminals, designated as emitter (E), base (B), and collector (C). For the *npn* transistor, the currents and voltages of the transistor are specified as in Fig. 3.39. Applying KCL to Fig. 3.39(a) gives

$$I_E = I_B + I_C \tag{3.27}$$

where I_E, I_C, and I_B are emitter, collector, and base currents, respectively. Similarly, applying KVL to Fig. 3.39(b) gives

$$V_{CE} + V_{EB} + V_{BC} = 0 \tag{3.28}$$

where V_{CE}, V_{EB}, and V_{BC} are collector-emitter, emitter-base, and base-collector voltages. The BJT can operate in one of three modes: active, cutoff, and saturation. When transistors operate in the active mode, typically $V_{BE} \simeq 0.7$ V,

$$I_C = \alpha I_E \tag{3.29}$$

where α is called the *common-base current gain*. In Eq. (3.29), α denotes the fraction of electrons injected by the emitter that are collected by the collector. Also,

$$\boxed{I_C = \beta I_B} \tag{3.30}$$

where β is known as the *common-emitter current gain*. The α and β are characteristic properties of a given transistor and assume constant values for that transistor. Typically, α takes values in the range of 0.98 to 0.999, while β takes values in the range of 50 to 1000. From Eqs. (3.27) to (3.30), it is evident that

$$I_E = (1 + \beta)I_B \tag{3.31}$$

and

$$\beta = \frac{\alpha}{1 - \alpha} \tag{3.32}$$

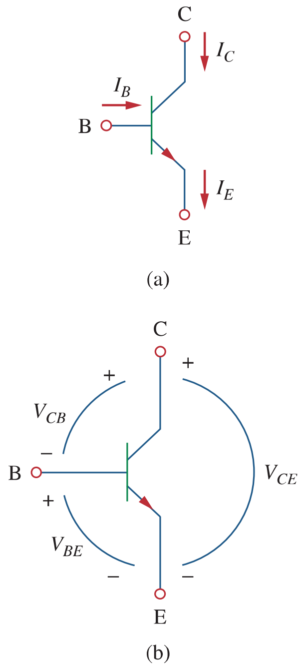


Figure 3.39
The terminal variables of an *npn* transistor: (a) currents, (b) voltages.

These equations show that, in the active mode, the BJT can be modeled as a dependent current-controlled current source. Thus, in circuit analysis, the dc equivalent model in Fig. 3.40(b) may be used to replace the *npn* transistor in Fig. 3.40(a). Since β in Eq. (3.32) is large, a small base current controls large currents in the output circuit. Consequently, the bipolar transistor can serve as an amplifier, producing both current gain and voltage gain. Such amplifiers can be used to furnish a considerable amount of power to transducers such as loudspeakers or control motors.

In fact, transistor circuits provide motivation to study dependent sources.

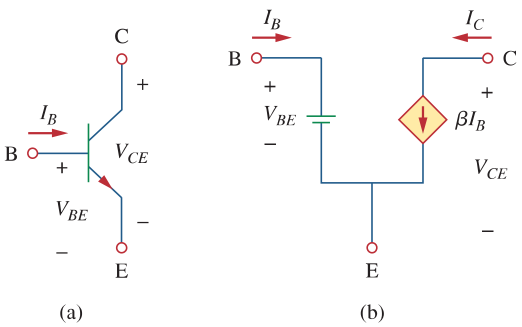


Figure 3.40
(a) An *npn* transistor, (b) its dc equivalent model.

It should be observed in the following examples that one cannot directly analyze transistor circuits using nodal analysis because of the potential difference between the terminals of the transistor. Only when the transistor is replaced by its equivalent model can we apply nodal analysis.

Example 3.12

Find I_B, I_C, and v_o in the transistor circuit of Fig. 3.41. Assume that the transistor operates in the active mode and that $\beta = 50$.

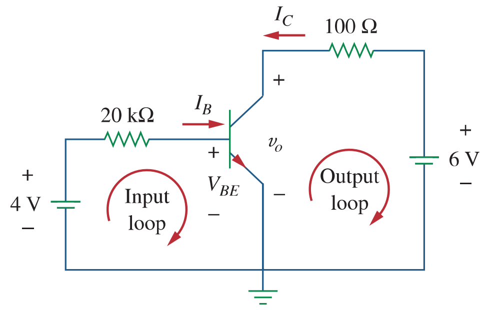


Figure 3.41
For Example 3.12.

Solution:
For the input loop, KVL gives

$$-4 + I_B(20 \times 10^3) + V_{BE} = 0$$

Since $V_{BE} = 0.7$ V in the active mode,

$$I_B = \frac{4 - 0.7}{20 \times 10^3} = 165\ \mu\text{A}$$

But

$$I_C = \beta I_B = 50 \times 165\ \mu\text{A} = 8.25\ \text{mA}$$

For the output loop, KVL gives

$$-v_o - 100I_C + 6 = 0$$

or

$$v_o = 6 - 100I_C = 6 - 0.825 = 5.175\ \text{V}$$

Note that $v_o = V_{CE}$ in this case.

Practice Problem 3.12

For the transistor circuit in Fig. 3.42, let $\beta = 100$ and $V_{BE} = 0.7$ V. Determine v_o and V_{CE}.

Answer: 2.876 V, 1.984 V.

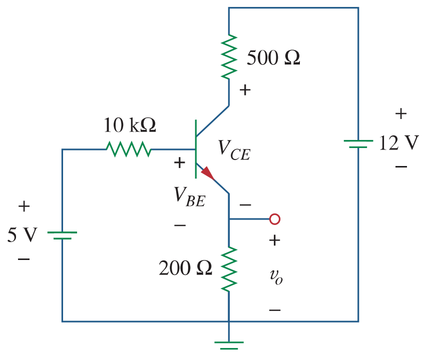


Figure 3.42
For Practice Prob. 3.12.

Example 3.13

For the BJT circuit in Fig. 3.43, $\beta = 150$ and $V_{BE} = 0.7$ V. Find v_o.

Solution:

1. **Define.** The circuit is clearly defined and the problem is clearly stated. There appear to be no additional questions that need to be asked.
2. **Present.** We are to determine the output voltage of the circuit shown in Fig. 3.43. The circuit contains an ideal transistor with $\beta = 150$ and $V_{BE} = 0.7$ V.
3. **Alternative.** We can use mesh analysis to solve for v_o. We can replace the transistor with its equivalent circuit and use nodal analysis. We can try both approaches and use them to check each other. As a third check, we can use the equivalent circuit and solve it using *PSpice*.
4. **Attempt.**

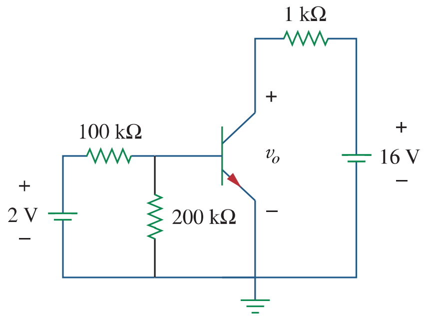


Figure 3.43
For Example 3.13.

METHOD 1 Working with Fig. 3.44(a), we start with the first loop.

$$-2 + 100\text{k}I_1 + 200\text{k}(I_1 - I_2) = 0 \qquad \text{or} \qquad 3I_1 - 2I_2 = 2 \times 10^{-5} \tag{3.13.1}$$

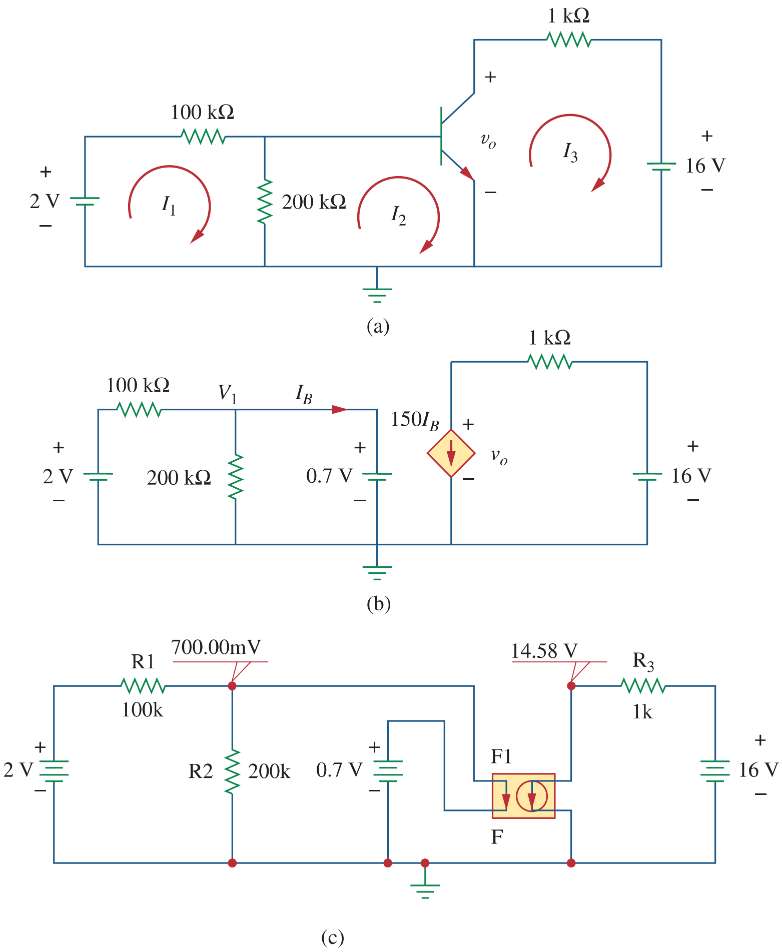


Figure 3.44
Solution of the problem in Example 3.13: (a) Method 1, (b) Method 2, (c) Method 3.

Now for loop 2.

$$200\text{k}(I_2 - I_1) + V_{BE} = 0 \qquad \text{or} \qquad -2I_1 + 2I_2 = -0.7 \times 10^{-5} \tag{3.13.2}$$

Since we have two equations and two unknowns, we can solve for I_1 and I_2. Adding Eq. (3.13.1) to (3.13.2) we get;

$$I_1 = 1.3 \times 10^{-5}\text{A} \qquad \text{and} \qquad I_2 = (-0.7 + 2.6)10^{-5}/2 = 9.5\ \mu\text{A}$$

Since $I_3 = -150I_2 = -1.425$ mA, we can now solve for v_o using loop 3:

$$-v_o + {}^{1}\text{k}I_3 + 16 = 0 \qquad \text{or} \qquad v_o = -1.425 + 16 = \mathbf{14.575\ V}$$

METHOD 2 Replacing the transistor with its equivalent circuit produces the circuit shown in Fig. 3.44(b). We can now use nodal analysis to solve for v_o.

At node number 1: $V_1 = 0.7$ V

$$(0.7 - 2)/100\text{k} + 0.7/200\text{k} + I_B = 0 \qquad \text{or} \qquad I_B = 9.5\ \mu\text{A}$$

At node number 2 we have:

$$150I_B + (v_o - 16)/1\text{k} = 0 \qquad \text{or}$$
$$v_o = 16 - 150 \times 10^3 \times 9.5 \times 10^{-6} = \mathbf{14.575\ V}$$

5. **Evaluate.** The answers check, but to further check we can use *PSpice* (Method 3), which gives us the solution shown in Fig. 3.44(c).
6. **Satisfactory?** Clearly, we have obtained the desired answer with a very high confidence level. We can now present our work as a solution to the problem.

Practice Problem 3.13

The transistor circuit in Fig. 3.45 has $\beta = 80$ and $V_{BE} = 0.7$ V. Find v_o and I_o.

Answer: 12 V, 600 μA.

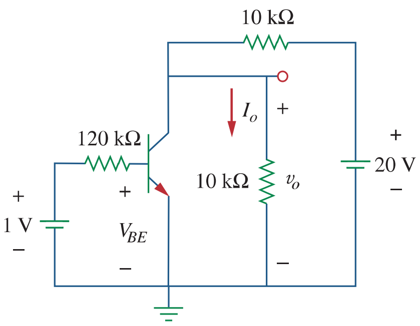


Figure 3.45
For Practice Prob. 3.13.

3.10 Summary

1. Nodal analysis is the application of Kirchhoff's current law at the nonreference nodes. (It is applicable to both planar and nonplanar circuits.) We express the result in terms of the node voltages. Solving the simultaneous equations yields the node voltages.
2. A supernode consists of two nonreference nodes connected by a (dependent or independent) voltage source.
3. Mesh analysis is the application of Kirchhoff's voltage law around meshes in a planar circuit. We express the result in terms of mesh currents. Solving the simultaneous equations yields the mesh currents.

4. A supermesh consists of two meshes that have a (dependent or independent) current source in common.
5. Nodal analysis is normally used when a circuit has fewer node equations than mesh equations. Mesh analysis is normally used when a circuit has fewer mesh equations than node equations.
6. Circuit analysis can be carried out using *PSpice*.
7. DC transistor circuits can be analyzed using the techniques covered in this chapter.

Review Questions

3.1 At node 1 in the circuit of Fig. 3.46, applying KCL gives:

(a) $2 + \dfrac{12 - v_1}{3} = \dfrac{v_1}{6} + \dfrac{v_1 - v_2}{4}$

(b) $2 + \dfrac{v_1 - 12}{3} = \dfrac{v_1}{6} + \dfrac{v_2 - v_1}{4}$

(c) $2 + \dfrac{12 - v_1}{3} = \dfrac{0 - v_1}{6} + \dfrac{v_1 - v_2}{4}$

(d) $2 + \dfrac{v_1 - 12}{3} = \dfrac{0 - v_1}{6} + \dfrac{v_2 - v_1}{4}$

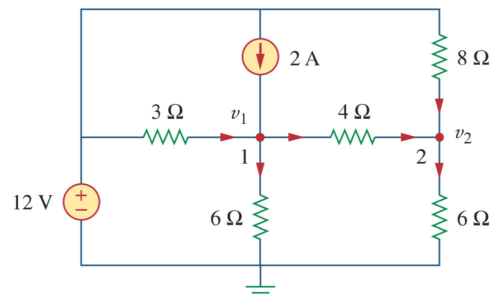


Figure 3.46
For Review Questions 3.1 and 3.2.

3.2 In the circuit of Fig. 3.46, applying KCL at node 2 gives:

(a) $\dfrac{v_2 - v_1}{4} + \dfrac{v_2}{8} = \dfrac{v_2}{6}$

(b) $\dfrac{v_1 - v_2}{4} + \dfrac{v_2}{8} = \dfrac{v_2}{6}$

(c) $\dfrac{v_1 - v_2}{4} + \dfrac{12 - v_2}{8} = \dfrac{v_2}{6}$

(d) $\dfrac{v_2 - v_1}{4} + \dfrac{v_2 - 12}{8} = \dfrac{v_2}{6}$

3.3 For the circuit in Fig. 3.47, v_1 and v_2 are related as:

(a) $v_1 = 6i + 8 + v_2$ (b) $v_1 = 6i - 8 + v_2$
(c) $v_1 = -6i + 8 + v_2$ (d) $v_1 = -6i - 8 + v_2$

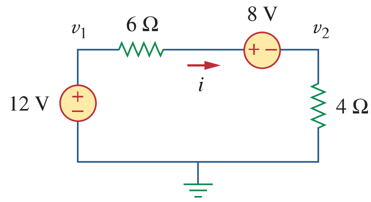


Figure 3.47
For Review Questions 3.3 and 3.4.

3.4 In the circuit of Fig. 3.47, the voltage v_2 is:

(a) −8 V (b) −1.6 V
(c) 1.6 V (d) 8 V

3.5 The current i in the circuit of Fig. 3.48 is:

(a) −2.667 A (b) −0.667 A
(c) 0.667 A (d) 2.667 A

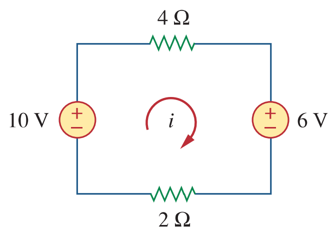


Figure 3.48
For Review Questions 3.5 and 3.6.

3.6 The loop equation for the circuit in Fig. 3.48 is:

(a) $-10 + 4i + 6 + 2i = 0$
(b) $10 + 4i + 6 + 2i = 0$
(c) $10 + 4i - 6 + 2i = 0$
(d) $-10 + 4i - 6 + 2i = 0$

3.7 In the circuit of Fig. 3.49, current i_1 is:

(a) 4 A (b) 3 A (c) 2 A (d) 1 A

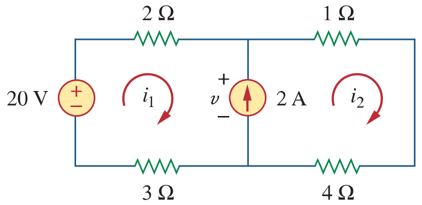


Figure 3.49
For Review Questions 3.7 and 3.8.

3.8 The voltage v across the current source in the circuit of Fig. 3.49 is:

(a) 20 V (b) 15 V (c) 10 V (d) 5 V

3.9 The *PSpice* part name for a current-controlled voltage source is:

(a) EX (b) FX (c) HX (d) GX

3.10 Which of the following statements are not true of the pseudocomponent IPROBE:

(a) It must be connected in series.
(b) It plots the branch current.
(c) It displays the current through the branch in which it is connected.
(d) It can be used to display voltage by connecting it in parallel.
(e) It is used only for dc analysis.
(f) It does not correspond to a particular circuit element.

Answers: 3.1a, 3.2c, 3.3a, 3.4c, 3.5c, 3.6a, 3.7d, 3.8b, 3.9c, 3.10b,d.

Problems

Sections 3.2 and 3.3 Nodal Analysis

3.1 Using Fig. 3.50, design a problem to help other students better understand nodal analysis.

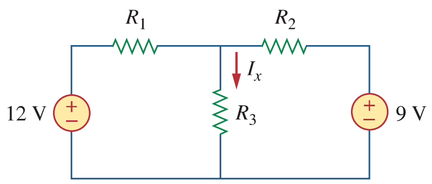


Figure 3.50
For Prob. 3.1 and Prob. 3.39.

3.2 For the circuit in Fig. 3.51, obtain v_1 and v_2.

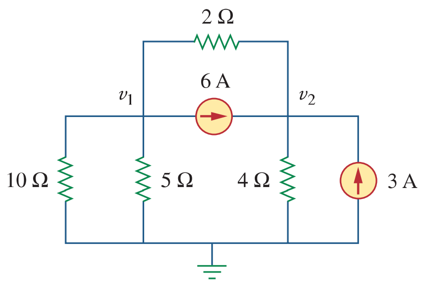


Figure 3.51
For Prob. 3.2.

3.3 Find the currents I_1 through I_4 and the voltage v_o in the circuit of Fig. 3.52.

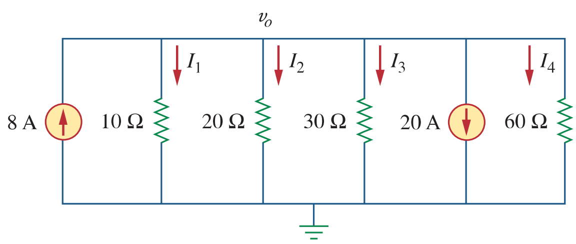


Figure 3.52
For Prob. 3.3.

3.4 Given the circuit in Fig. 3.53, calculate the currents i_1 through i_4.

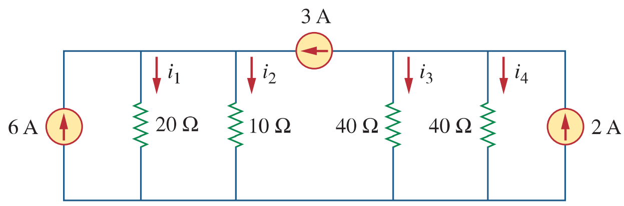


Figure 3.53
For Prob. 3.4.

3.5 Obtain v_o in the circuit of Fig. 3.54.

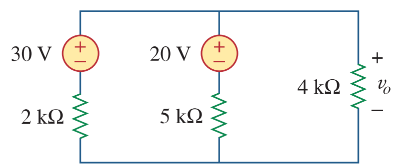


Figure 3.54
For Prob. 3.5.

3.6 Solve for V_1 in the circuit of Fig. 3.55 using nodal analysis.

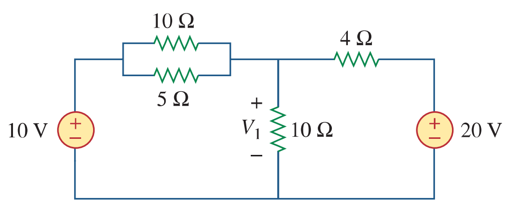


Figure 3.55
For Prob. 3.6.

3.7 Apply nodal analysis to solve for V_x in the circuit of Fig. 3.56.

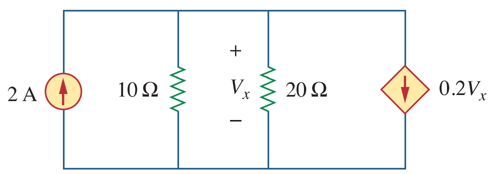


Figure 3.56
For Prob. 3.7.

3.8 Using nodal analysis, find v_o in the circuit of Fig. 3.57.

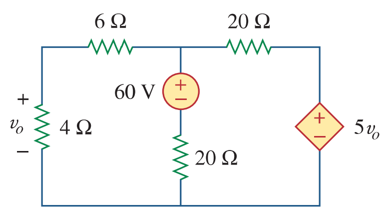


Figure 3.57
For Prob. 3.8 and Prob. 3.37.

3.9 Determine I_b in the circuit in Fig. 3.58 using nodal analysis.

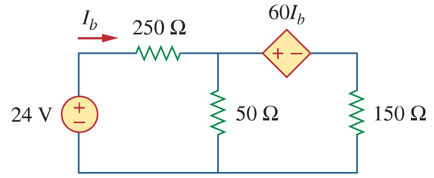


Figure 3.58
For Prob. 3.9.

3.10 Find I_o in the circuit of Fig. 3.59.

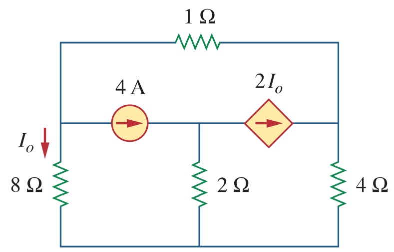


Figure 3.59
For Prob. 3.10.

3.11 Find V_o and the power dissipated in all the resistors in the circuit of Fig. 3.60.

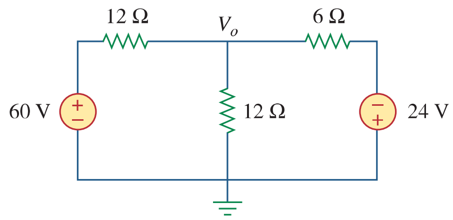


Figure 3.60
For Prob. 3.11.

3.12 Using nodal analysis, determine V_o in the circuit in Fig. 3.61.

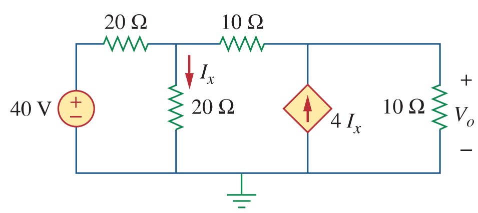


Figure 3.61
For Prob. 3.12.

3.13 Calculate v_1 and v_2 in the circuit of Fig. 3.62 using nodal analysis.

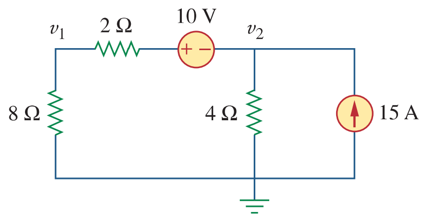


Figure 3.62
For Prob. 3.13.

3.14 Using nodal analysis, find v_o in the circuit of Fig. 3.63.

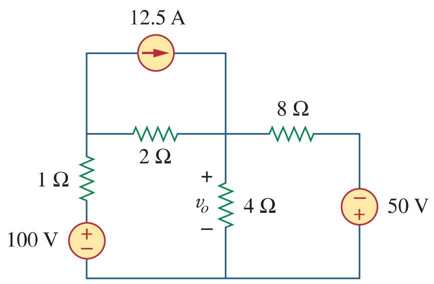


Figure 3.63
For Prob. 3.14.

3.15 Apply nodal analysis to find i_o and the power dissipated in each resistor in the circuit of Fig. 3.64.

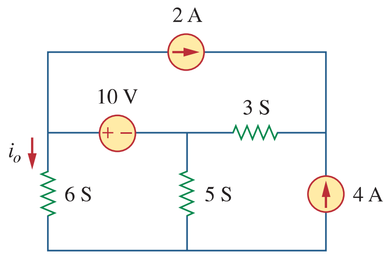


Figure 3.64
For Prob. 3.15.

3.16 Determine voltages v_1 through v_3 in the circuit of Fig. 3.65 using nodal analysis.

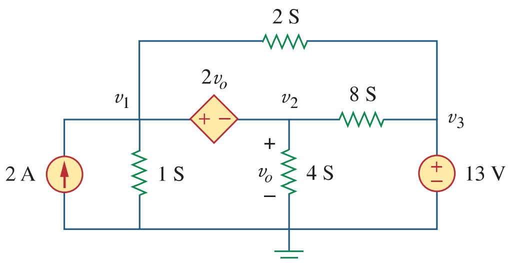


Figure 3.65
For Prob. 3.16.

3.17 Using nodal analysis, find current i_o in the circuit of Fig. 3.66.

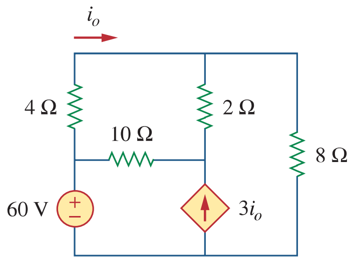


Figure 3.66
For Prob. 3.17.

3.18 Determine the node voltages in the circuit in Fig. 3.67 using nodal analysis.

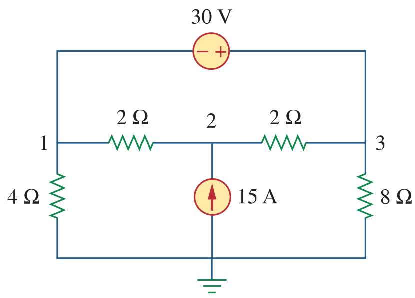


Figure 3.67
For Prob. 3.18.

3.19 Use nodal analysis to find v_1, v_2, and v_3 in the circuit of Fig. 3.68.

ML

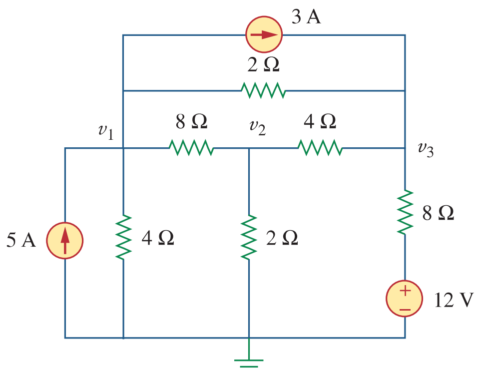


Figure 3.68
For Prob. 3.19.

3.20 For the circuit in Fig. 3.69, find v_1, v_2, and v_3 using nodal analysis.

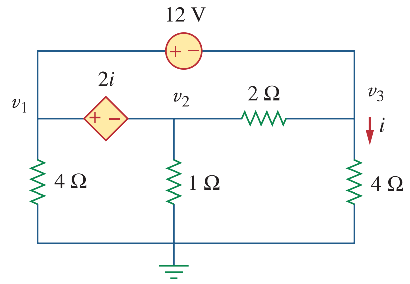


Figure 3.69
For Prob. 3.20.

3.21 For the circuit in Fig. 3.70, find v_1 and v_2 using nodal analysis.

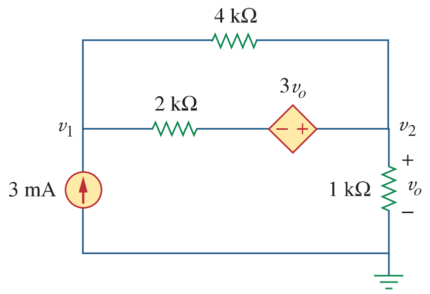


Figure 3.70
For Prob. 3.21.

3.22 Determine v_1 and v_2 in the circuit of Fig. 3.71.

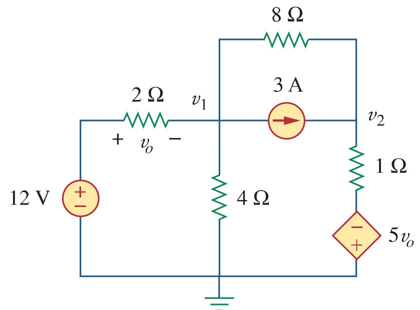


Figure 3.71
For Prob. 3.22.

3.23 Use nodal analysis to find V_o in the circuit of Fig. 3.72.

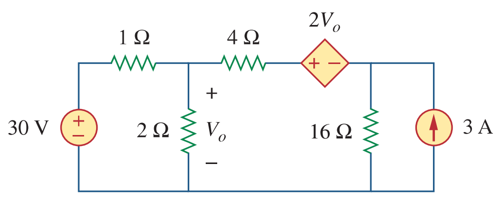


Figure 3.72
For Prob. 3.23.

3.24 Use nodal analysis and *MATLAB* to find V_o in the circuit of Fig. 3.73.
ML

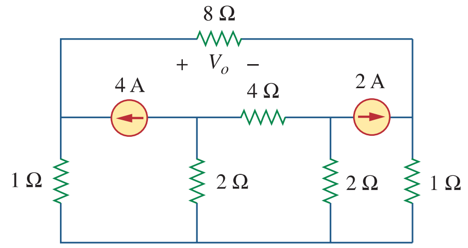


Figure 3.73
For Prob. 3.24.

3.25 Use nodal analysis along with *MATLAB* to determine the node voltages in Fig. 3.74.
ML

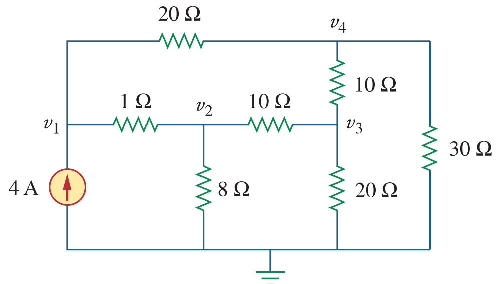


Figure 3.74
For Prob. 3.25.

3.26 Calculate the node voltages v_1, v_2, and v_3 in the circuit of Fig. 3.75.
ML

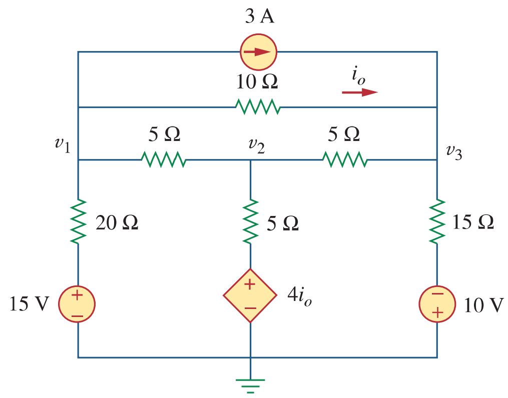


Figure 3.75
For Prob. 3.26.

***3.27** Use nodal analysis to determine voltages v_1, v_2, and v_3 in the circuit of Fig. 3.76.

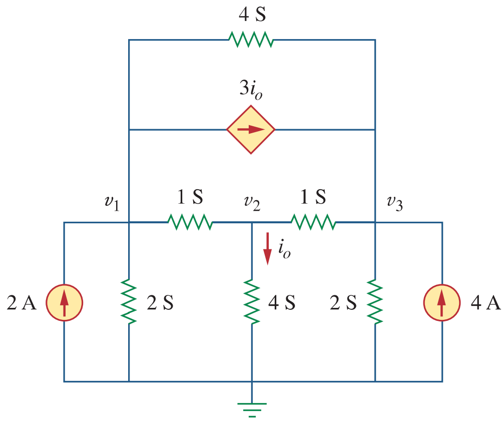


Figure 3.76
For Prob. 3.27.

***3.28** Use *MATLAB* to find the voltages at nodes *a*, *b*, *c*, and *d* in the circuit of Fig. 3.77.

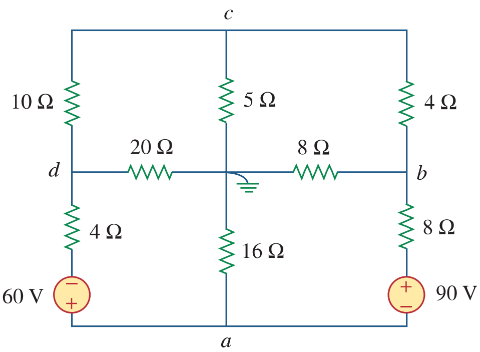


Figure 3.77
For Prob. 3.28.

3.29 Use *MATLAB* to solve for the node voltages in the circuit of Fig. 3.78.

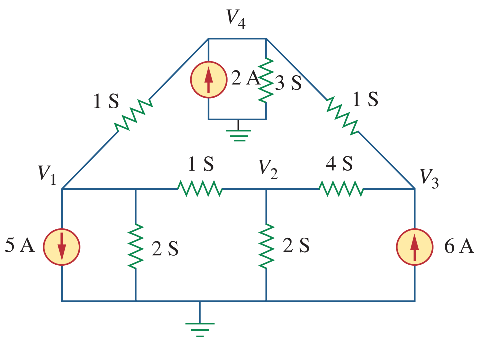


Figure 3.78
For Prob. 3.29.

* An asterisk indicates a challenging problem.

3.30 Using nodal analysis, find v_o and i_o in the circuit of Fig. 3.79.

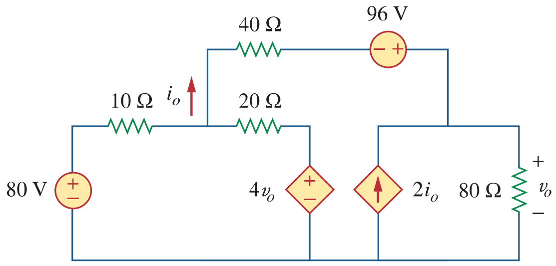


Figure 3.79
For Prob. 3.30.

3.31 Find the node voltages for the circuit in Fig. 3.80.

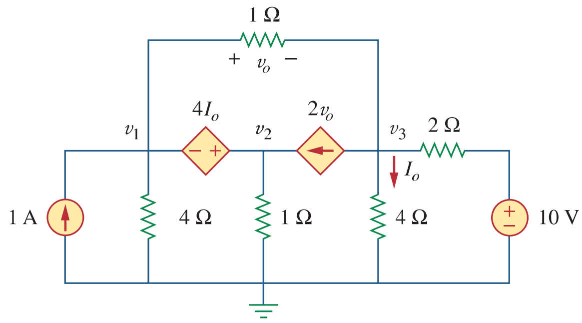


Figure 3.80
For Prob. 3.31.

3.32 Obtain the node voltages v_1, v_2, and v_3 in the circuit of Fig. 3.81.

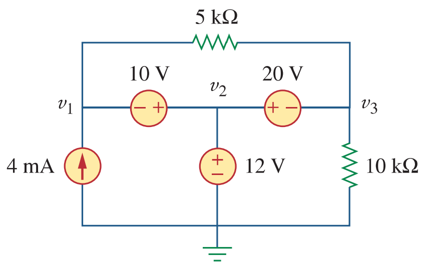


Figure 3.81
For Prob. 3.32.

Sections 3.4 and 3.5 Mesh Analysis

3.33 Which of the circuits in Fig. 3.82 is planar? For the planar circuit, redraw the circuits with no crossing branches.

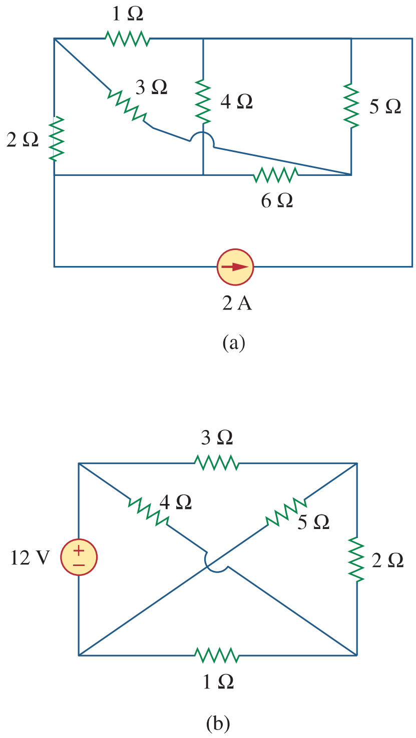
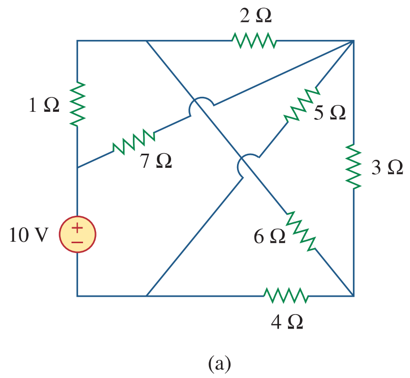


Figure 3.82
For Prob. 3.33.

3.34 Determine which of the circuits in Fig. 3.83 is planar and redraw it with no crossing branches.



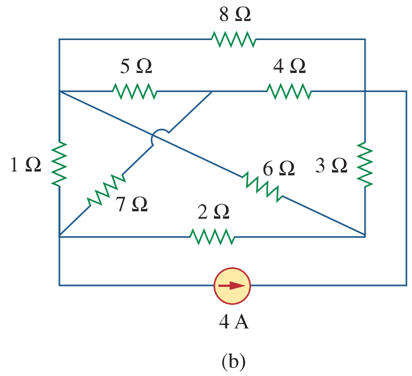


Figure 3.83
For Prob. 3.34.

3.35 Rework Prob. 3.5 using mesh analysis.

3.36 Use mesh analysis to obtain i_1, i_2, and i_3 in the circuit in Fig. 3.84.

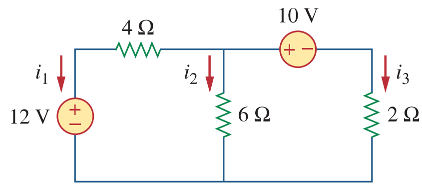


Figure 3.84
For Prob. 3.36.

3.37 Solve Prob. 3.8 using mesh analysis.

3.38 Apply mesh analysis to the circuit in Fig. 3.85 and obtain I_o.
ML

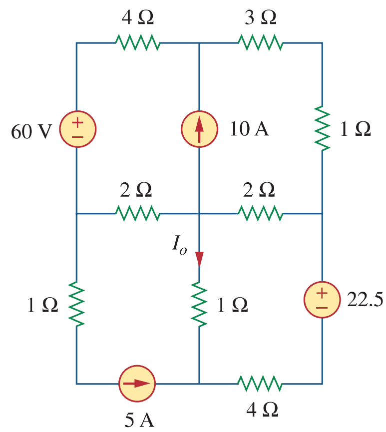


Figure 3.85
For Prob. 3.38.

3.39 Using Fig. 3.50 from Prob. 3.1, design a problem to help other students better understand mesh analysis.

3.40 For the bridge network in Fig. 3.86, find i_o using mesh analysis.

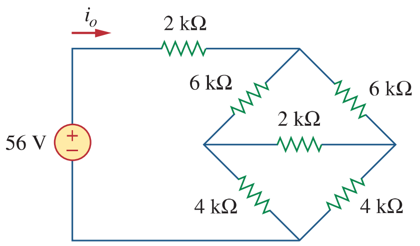


Figure 3.86
For Prob. 3.40.

3.41 Apply mesh analysis to find i in Fig. 3.87.

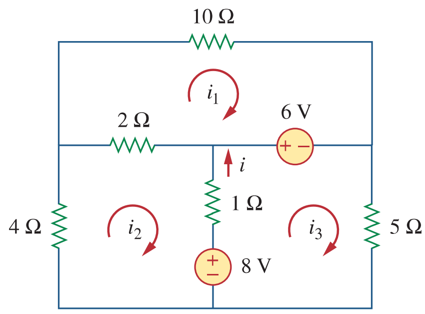


Figure 3.87
For Prob. 3.41.

3.42 Using Fig. 3.88, design a problem to help students better understand mesh analysis using matrices.

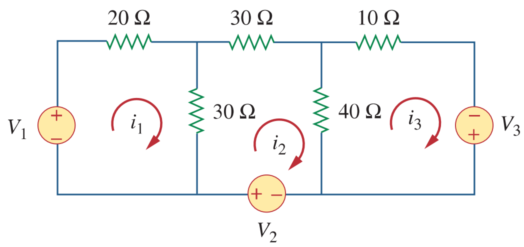


Figure 3.88
For Prob. 3.42.

3.43 Use mesh analysis to find v_{ab} and i_o in the circuit of Fig. 3.89.

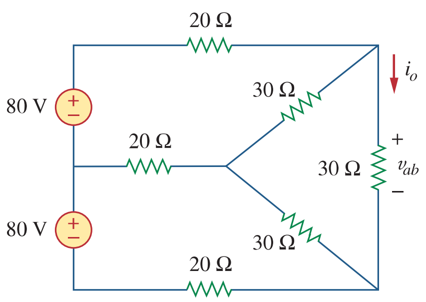


Figure 3.89
For Prob. 3.43.

3.44 Use mesh analysis to obtain i_o in the circuit of Fig. 3.90.

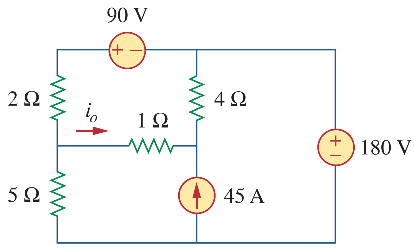


Figure 3.90
For Prob. 3.44.

3.45 Find current i in the circuit of Fig. 3.91.

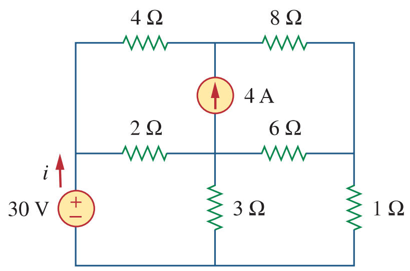


Figure 3.91
For Prob. 3.45.

3.46 Calculate the mesh currents i_1 and i_2 in Fig. 3.92.

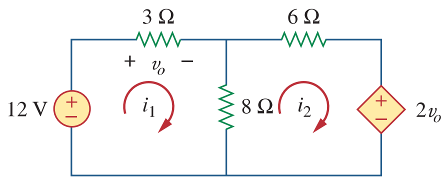


Figure 3.92
For Prob. 3.46.

3.47 Rework Prob. 3.19 using mesh analysis.

3.48 Determine the current through the 10-kΩ resistor in the circuit of Fig. 3.93 using mesh analysis.

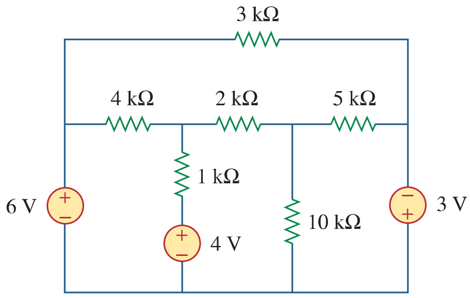


Figure 3.93
For Prob. 3.48.

3.49 Find v_o and i_o in the circuit of Fig. 3.94.

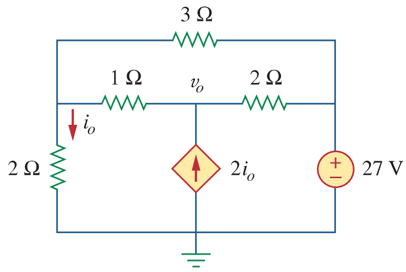


Figure 3.94
For Prob. 3.49.

3.50 Use mesh analysis to find the current i_o in the circuit of Fig. 3.95.

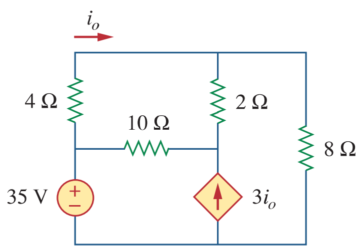


Figure 3.95
For Prob. 3.50.

3.51 Apply mesh analysis to find v_o in the circuit of Fig. 3.96.

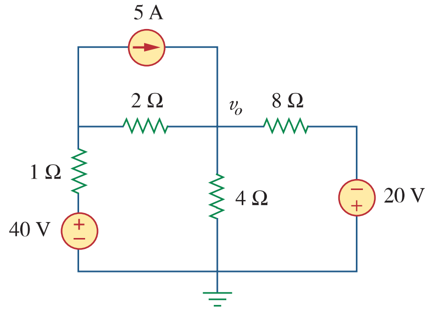


Figure 3.96
For Prob. 3.51.

3.52 Use mesh analysis to find i_1, i_2, and i_3 in the circuit of Fig. 3.97.

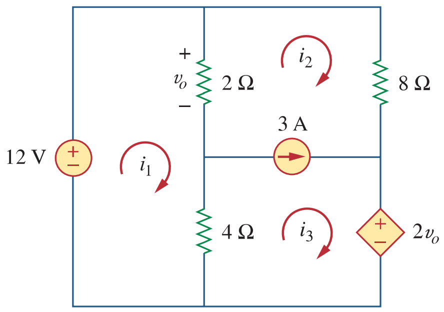


Figure 3.97
For Prob. 3.52.

3.53 Find the mesh currents in the circuit of Fig. 3.98 using *MATLAB*.

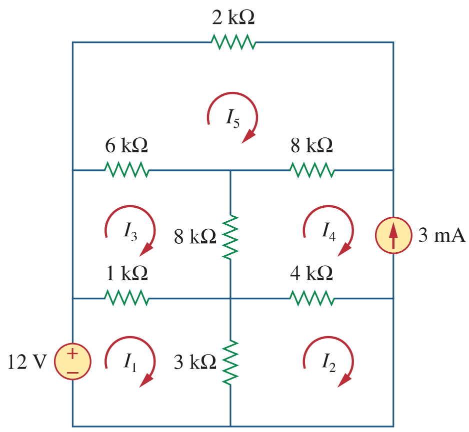


Figure 3.98
For Prob. 3.53.

3.54 Find the mesh currents i_1, i_2, and i_3 in the circuit in Fig. 3.99.

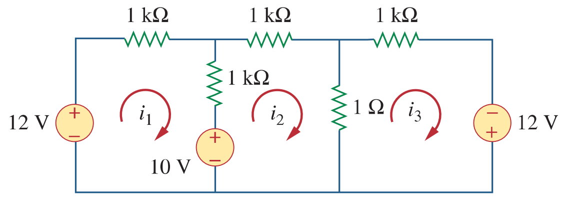


Figure 3.99
For Prob. 3.54.

***3.55** In the circuit of Fig. 3.100, solve for I_1, I_2, and I_3.

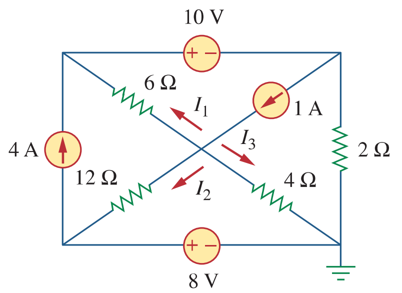


Figure 3.100
For Prob. 3.55.

3.56 Determine v_1 and v_2 in the circuit of Fig. 3.101.

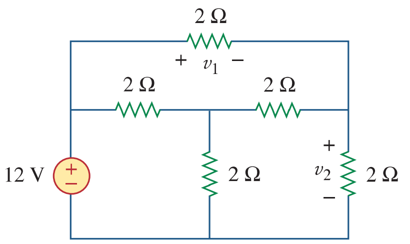


Figure 3.101
For Prob. 3.56.

3.57 In the circuit of Fig. 3.102, find the values of R, V_1, and V_2 given that $i_o = 15$ mA.

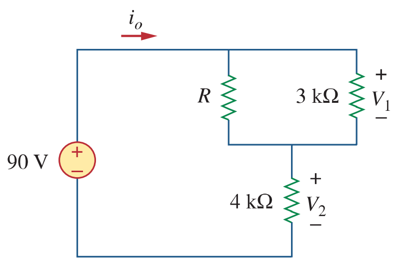


Figure 3.102
For Prob. 3.57.

3.58 Find i_1, i_2, and i_3 in the circuit of Fig. 3.103.

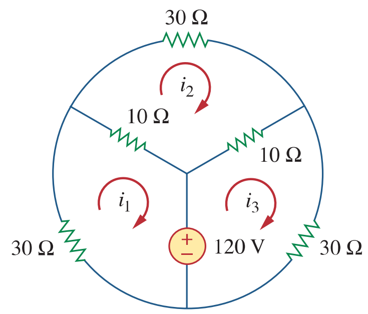


Figure 3.103
For Prob. 3.58.

3.59 Rework Prob. 3.30 using mesh analysis.

3.60 Calculate the power dissipated in each resistor in the circuit of Fig. 3.104.

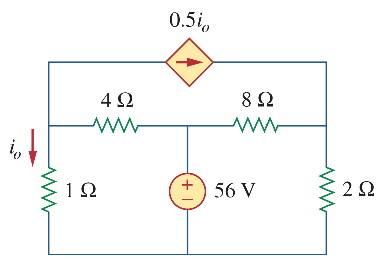


Figure 3.104
For Prob. 3.60.

3.61 Calculate the current gain i_o/i_s in the circuit of Fig. 3.105.

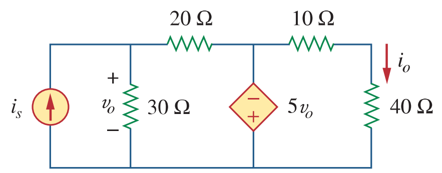


Figure 3.105
For Prob. 3.61.

3.62 Find the mesh currents i_1, i_2, and i_3 in the network of Fig. 3.106.

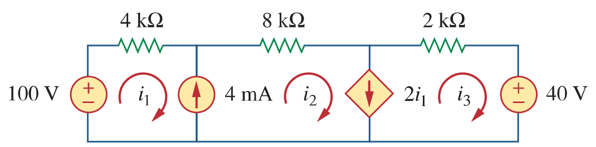


Figure 3.106
For Prob. 3.62.

3.63 Find v_x and i_x in the circuit shown in Fig. 3.107.

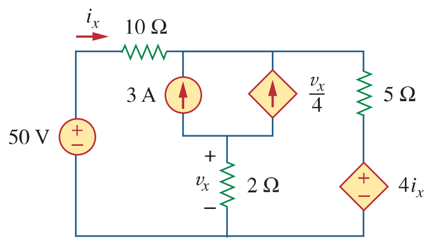


Figure 3.107
For Prob. 3.63.

3.64 Find v_o and i_o in the circuit of Fig. 3.108.

ML

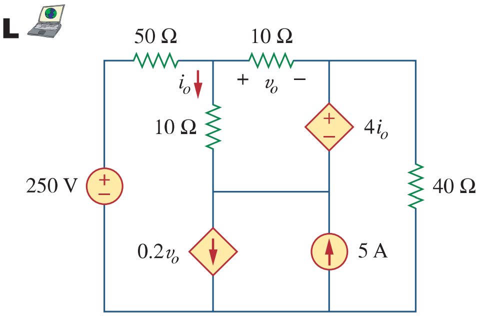


Figure 3.108
For Prob. 3.64.

3.65 Use *MATLAB* to solve for the mesh currents in the circuit of Fig. 3.109.

ML

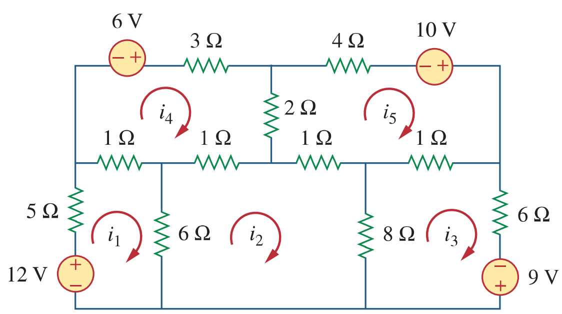


Figure 3.109
For Prob. 3.65.

3.66 Write a set of mesh equations for the circuit in Fig. 3.110. Use *MATLAB* to determine the mesh currents.

ML

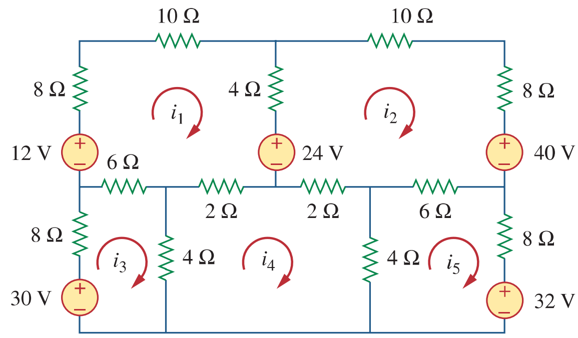


Figure 3.110
For Prob. 3.66.

Section 3.6 Nodal and Mesh Analyses by Inspection

3.67 Obtain the node-voltage equations for the circuit in Fig. 3.111 by inspection. Then solve for V_o.

ML

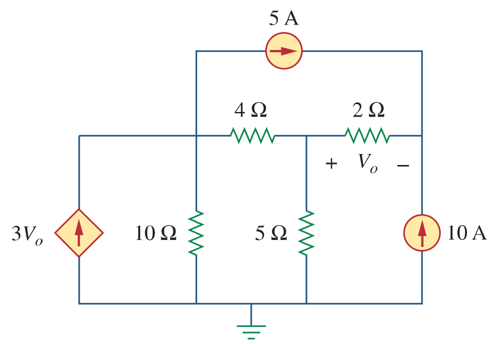


Figure 3.111
For Prob. 3.67.

3.68 Using Fig. 3.112, design a problem, to solve for V_o, to help other students better understand nodal analysis. Try your best to come up with values to make the calculations easier.

e2d

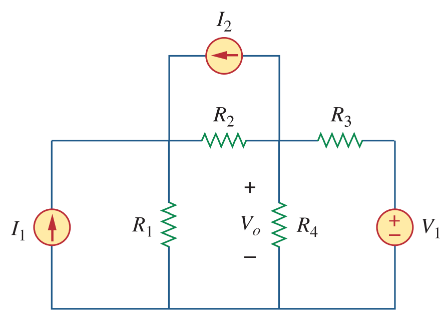


Figure 3.112
For Prob. 3.68.

3.69 For the circuit shown in Fig. 3.113, write the node-voltage equations by inspection.

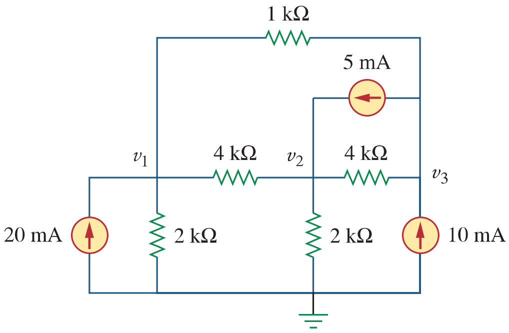


Figure 3.113
For Prob. 3.69.

3.70 Write the node-voltage equations by inspection and then determine values of V_1 and V_2 in the circuit of Fig. 3.114.

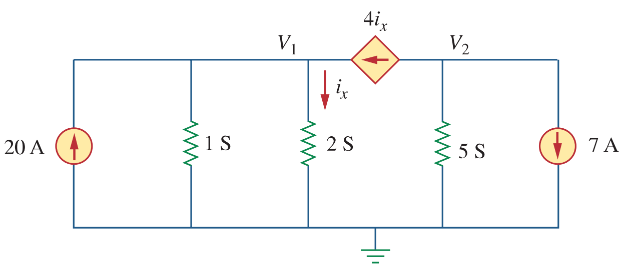


Figure 3.114
For Prob. 3.70.

3.71 Write the mesh-current equations for the circuit in Fig. 3.115. Next, determine the values of i_1, i_2, and i_3.

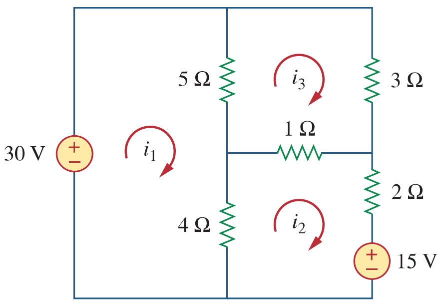


Figure 3.115
For Prob. 3.71.

3.72 By inspection, write the mesh-current equations for the circuit in Fig. 3.116.

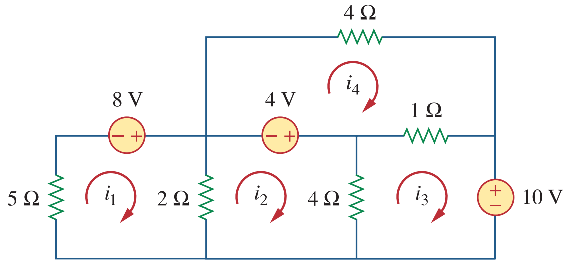


Figure 3.116
For Prob. 3.72.

3.73 Write the mesh-current equations for the circuit in Fig. 3.117.

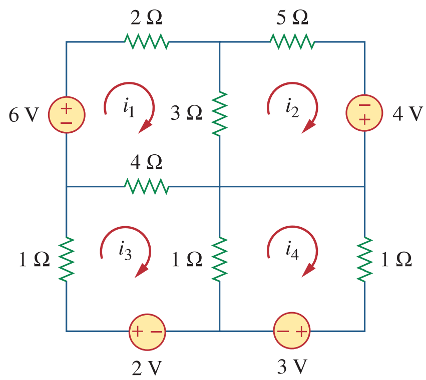


Figure 3.117
For Prob. 3.73.

3.74 By inspection, obtain the mesh-current equations for the circuit in Fig. 3.118.

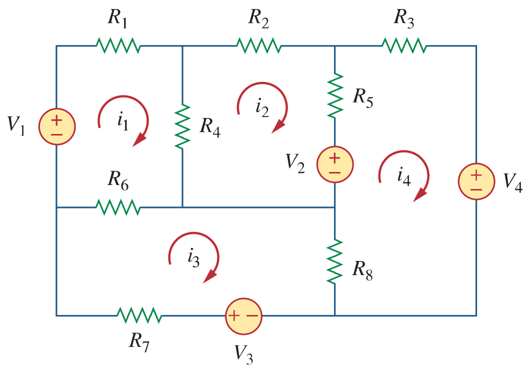


Figure 3.118
For Prob. 3.74.

Section 3.8 Circuit Analysis with *PSpice* or *MultiSim*

3.75 Use *PSpice* or *MultiSim* to solve Prob. 3.58.

3.76 Use *PSpice* or *MultiSim* to solve Prob. 3.27.

3.77 Solve for V_1 and V_2 in the circuit of Fig. 3.119 using *PSpice* or *MultiSim*.

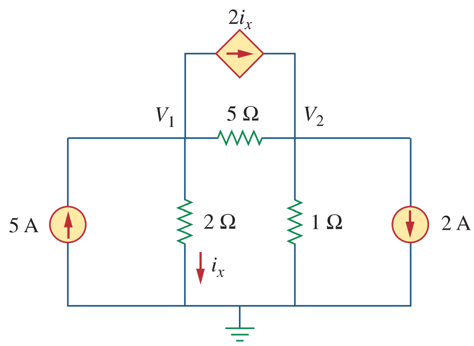


Figure 3.119
For Prob. 3.77.

3.78 Solve Prob. 3.20 using *PSpice* or *MultiSim*.

3.79 Rework Prob. 3.28 using *PSpice* or *MultiSim*.

3.80 Find the nodal voltages v_1 through v_4 in the circuit of Fig. 3.120 using *PSpice* or *MultiSim*.

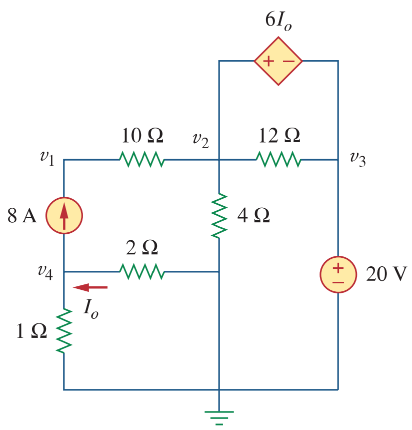


Figure 3.120
For Prob. 3.80.

3.81 Use *PSpice* or *MultiSim* to solve the problem in Example 3.4.

3.82 If the Schematics Netlist for a network is as follows, draw the network.

```
R_R1   1  2  2K
R_R2   2  0  4K
R_R3   3  0  8K
R_R4   3  4  6K
R_R5   1  3  3K
V_VS   4  0  DC     100
I_IS   0  1  DC     4
F_F1   1  3  VF_F1  2
VF_F1  5  0  0V
E_E1   3  2  1      3     3
```

3.83 The following program is the Schematics Netlist of a particular circuit. Draw the circuit and determine the voltage at node 2.

```
R_R1  1  2  20
R_R2  2  0  50
R_R3  2  3  70
R_R4  3  0  30
V_VS  1  0  20V
I_IS  2  0  DC   2A
```

Section 3.9 Applications

3.84 Calculate v_o and I_o in the circuit of Fig. 3.121.

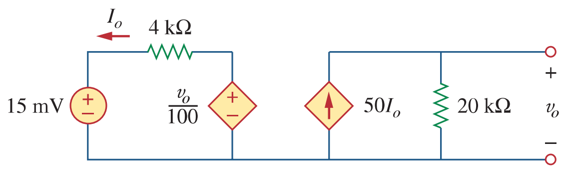


Figure 3.121
For Prob. 3.84.

3.85 An audio amplifier with a resistance of 9 Ω supplies power to a speaker. What should be the resistance of the speaker for maximum power to be delivered?

3.86 For the simplified transistor circuit of Fig. 3.122, calculate the voltage v_o.

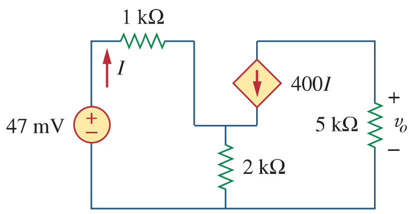


Figure 3.122
For Prob. 3.86.

3.87 For the circuit in Fig. 3.123, find the gain v_o/v_s.

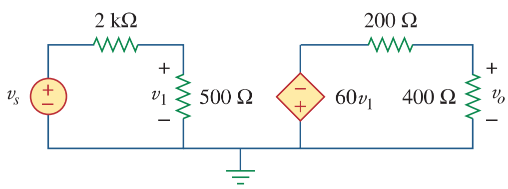


Figure 3.123
For Prob. 3.87.

***3.88** Determine the gain v_o/v_s of the transistor amplifier circuit in Fig. 3.124.

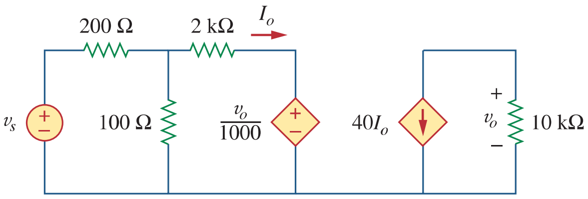


Figure 3.124
For Prob. 3.88.

3.89 For the transistor circuit shown in Fig. 3.125, find I_B and V_{CE}. Let $\beta = 100$, and $V_{BE} = 0.7$ V.

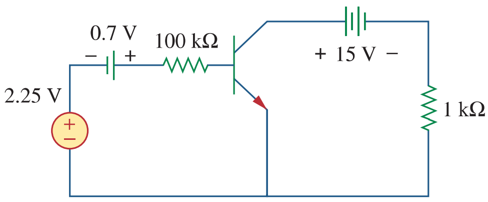


Figure 3.125
For Prob. 3.89.

3.90 Calculate v_s for the transistor in Fig. 3.126 given that $v_o = 4$ V, $\beta = 150$, $V_{BE} = 0.7$ V.

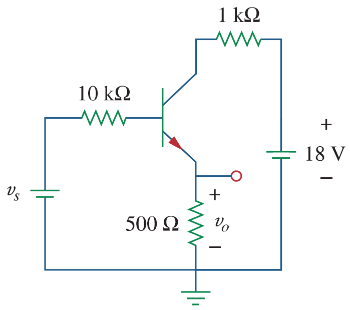


Figure 3.126
For Prob. 3.90.

3.91 For the transistor circuit of Fig. 3.127, find I_B, V_{CE}, and v_o. Take $\beta = 200$, $V_{BE} = 0.7$ V.

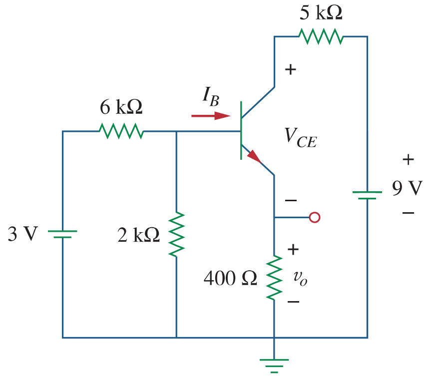


Figure 3.127
For Prob. 3.91.

3.92 Using Fig. 3.128, design a problem to help other students better understand transistors. Make sure you use reasonable numbers!

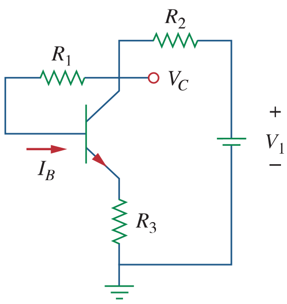


Figure 3.128
For Prob. 3.92.

Comprehensive Problem

***3.93** Rework Example 3.11 with hand calculation.

chapter

4

Circuit Theorems

Your success as an engineer will be directly proportional to your ability to communicate!

—Charles K. Alexander

Enhancing Your Skills and Your Career

Enhancing Your Communication Skills

Taking a course in circuit analysis is one step in preparing yourself for a career in electrical engineering. Enhancing your communication skills while in school should also be part of that preparation, as a large part of your time will be spent communicating.

People in industry have complained again and again that graduating engineers are ill-prepared in written and oral communication. An engineer who communicates effectively becomes a valuable asset.

You can probably speak or write easily and quickly. But how *effectively* do you communicate? The art of effective communication is of the utmost importance to your success as an engineer.

For engineers in industry, communication is key to promotability. Consider the result of a survey of U.S. corporations that asked what factors influence managerial promotion. The survey includes a listing of 22 personal qualities and their importance in advancement. You may be surprised to note that "technical skill based on experience" placed fourth from the bottom. Attributes such as self-confidence, ambition, flexibility, maturity, ability to make sound decisions, getting things done with and through people, and capacity for hard work all ranked higher. At the top of the list was "ability to communicate." The higher your professional career progresses, the more you will need to communicate. Therefore, you should regard effective communication as an important tool in your engineering tool chest.

Learning to communicate effectively is a lifelong task you should always work toward. The best time to begin is while still in school. Continually look for opportunities to develop and strengthen your reading, writing, listening, and speaking skills. You can do this through classroom presentations, team projects, active participation in student organizations, and enrollment in communication courses. The risks are less now than later in the workplace.

Ability to communicate effectively is regarded by many as the most important step to an executive promotion.
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4.1 Introduction

A major advantage of analyzing circuits using Kirchhoff's laws as we did in Chapter 3 is that we can analyze a circuit without tampering with its original configuration. A major disadvantage of this approach is that, for a large, complex circuit, tedious computation is involved.

The growth in areas of application of electric circuits has led to an evolution from simple to complex circuits. To handle the complexity, engineers over the years have developed some theorems to simplify circuit analysis. Such theorems include Thevenin's and Norton's theorems. Since these theorems are applicable to *linear* circuits, we first discuss the concept of circuit linearity. In addition to circuit theorems, we discuss the concepts of superposition, source transformation, and maximum power transfer in this chapter. The concepts we develop are applied in the last section to source modeling and resistance measurement.

4.2 Linearity Property

Linearity is the property of an element describing a linear relationship between cause and effect. Although the property applies to many circuit elements, we shall limit its applicability to resistors in this chapter. The property is a combination of both the homogeneity (scaling) property and the additivity property.

The homogeneity property requires that if the input (also called the *excitation*) is multiplied by a constant, then the output (also called the *response*) is multiplied by the same constant. For a resistor, for example, Ohm's law relates the input i to the output v,

$$v = iR \tag{4.1}$$

If the current is increased by a constant k, then the voltage increases correspondingly by k; that is,

$$\boxed{kiR = kv} \tag{4.2}$$

The additivity property requires that the response to a sum of inputs is the sum of the responses to each input applied separately. Using the voltage-current relationship of a resistor, if

$$v_1 = i_1 R \tag{4.3a}$$

and

$$v_2 = i_2 R \tag{4.3b}$$

then applying $(i_1 + i_2)$ gives

$$\boxed{v = (i_1 + i_2)R = i_1 R + i_2 R = v_1 + v_2} \tag{4.4}$$

We say that a resistor is a linear element because the voltage-current relationship satisfies both the homogeneity and the additivity properties.

In general, a circuit is linear if it is both additive and homogeneous. A linear circuit consists of only linear elements, linear dependent sources, and independent sources.

A **linear circuit** is one whose output is linearly related (or directly proportional) to its input.

Throughout this book we consider only linear circuits. Note that since $p = i^2R = v^2/R$ (making it a quadratic function rather than a linear one), the relationship between power and voltage (or current) is nonlinear. Therefore, the theorems covered in this chapter are not applicable to power.

To illustrate the linearity principle, consider the linear circuit shown in Fig. 4.1. The linear circuit has no independent sources inside it. It is excited by a voltage source v_s, which serves as the input. The circuit is terminated by a load R. We may take the current i through R as the output. Suppose $v_s = 10$ V gives $i = 2$ A. According to the linearity principle, $v_s = 1$ V will give $i = 0.2$ A. By the same token, $i = 1$ mA must be due to $v_s = 5$ mV.

For example, when current i_1 flows through resistor R, the power is $p_1 = Ri_1^2$, and when current i_2 flows through R, the power is $p_2 = Ri_2^2$. If current $i_1 + i_2$ flows through R, the power absorbed is $p_3 = R(i_1 + i_2)^2 = Ri_1^2 + Ri_2^2 + 2Ri_1i_2 \neq p_1 + p_2$. Thus, the power relation is nonlinear.

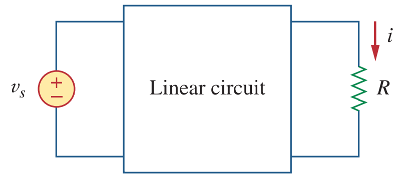

Figure 4.1
A linear circuit with input v_s and output i.

Example 4.1

For the circuit in Fig. 4.2, find I_o when $v_s = 12$ V and $v_s = 24$ V.

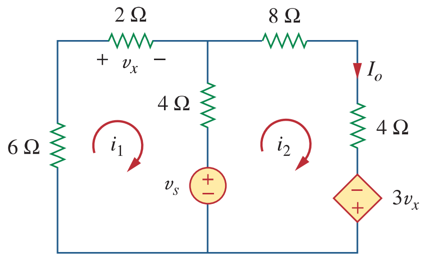

Figure 4.2
For Example 4.1.

Solution:
Applying KVL to the two loops, we obtain

$$12i_1 - 4i_2 + v_s = 0 \tag{4.1.1}$$

$$-4i_1 + 16i_2 - 3v_x - v_s = 0 \tag{4.1.2}$$

But $v_x = 2i_1$. Equation (4.1.2) becomes

$$-10i_1 + 16i_2 - v_s = 0 \tag{4.1.3}$$

Adding Eqs. (4.1.1) and (4.1.3) yields

$$2i_1 + 12i_2 = 0 \quad \Rightarrow \quad i_1 = -6i_2$$

Substituting this in Eq. (4.1.1), we get

$$-76i_2 + v_s = 0 \quad \Rightarrow \quad i_2 = \frac{v_s}{76}$$

When $v_s = 12$ V,

$$I_o = i_2 = \frac{12}{76} \text{ A}$$

When $v_s = 24$ V,

$$I_o = i_2 = \frac{24}{76} \text{ A}$$

showing that when the source value is doubled, I_o doubles.

Practice Problem 4.1

For the circuit in Fig. 4.3, find v_o when $i_s = 30$ and $i_s = 45$ A.

Answer: 40 V, 60 V.

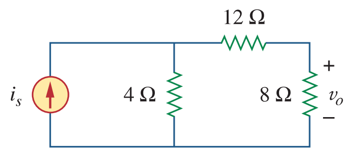

Figure 4.3
For Practice Prob. 4.1.

Example 4.2

Assume $I_o = 1$ A and use linearity to find the actual value of I_o in the circuit of Fig. 4.4.

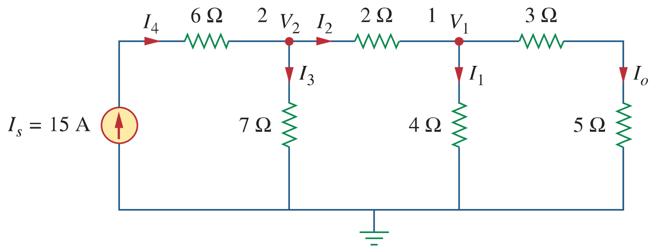

Figure 4.4
For Example 4.2.

Solution:
If $I_o = 1$ A, then $V_1 = (3 + 5)I_o = 8$ V and $I_1 = V_1/4 = 2$ A. Applying KCL at node 1 gives

$$I_2 = I_1 + I_o = 3 \text{ A}$$

$$V_2 = V_1 + 2I_2 = 8 + 6 = 14 \text{ V}, \qquad I_3 = \frac{V_2}{7} = 2 \text{ A}$$

Applying KCL at node 2 gives

$$I_4 = I_3 + I_2 = 5 \text{ A}$$

Therefore, $I_s = 5$ A. This shows that assuming $I_o = 1$ gives $I_s = 5$ A, the actual source current of 15 A will give $I_o = 3$ A as the actual value.

Practice Problem 4.2

Assume that $V_o = 1$ V and use linearity to calculate the actual value of V_o in the circuit of Fig. 4.5.

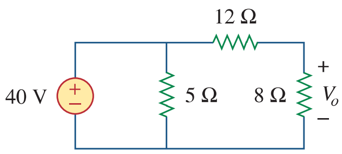

Figure 4.5
For Practice Prob. 4.2.

Answer: 16 V.

4.3 Superposition

If a circuit has two or more independent sources, one way to determine the value of a specific variable (voltage or current) is to use nodal or mesh analysis as in Chapter 3. Another way is to determine the contribution of each independent source to the variable and then add them up. The latter approach is known as the *superposition*.

The idea of superposition rests on the linearity property.

Superposition is not limited to circuit analysis but is applicable in many fields where cause and effect bear a linear relationship to one another.

> The **superposition** principle states that the voltage across (or current through) an element in a linear circuit is the algebraic sum of the voltages across (or currents through) that element due to each independent source acting alone.

The principle of superposition helps us to analyze a linear circuit with more than one independent source by calculating the contribution of each independent source separately. However, to apply the superposition principle, we must keep two things in mind:

1. We consider one independent source at a time while all other independent sources are *turned off*. This implies that we replace every voltage source by 0 V (or a short circuit), and every current source by 0 A (or an open circuit). This way we obtain a simpler and more manageable circuit.
2. Dependent sources are left intact because they are controlled by circuit variables.

Other terms such as *killed*, *made inactive*, *deadened*, or *set equal to zero* are often used to convey the same idea.

With these in mind, we apply the superposition principle in three steps:

Steps to Apply Superposition Principle:

1. Turn off all independent sources except one source. Find the output (voltage or current) due to that active source using the techniques covered in Chapters 2 and 3.
2. Repeat step 1 for each of the other independent sources.
3. Find the total contribution by adding algebraically all the contributions due to the independent sources.

Analyzing a circuit using superposition has one major disadvantage: It may very likely involve more work. If the circuit has three independent sources, we may have to analyze three simpler circuits each providing the contribution due to the respective individual source. However, superposition does help reduce a complex circuit to simpler circuits through replacement of voltage sources by short circuits and of current sources by open circuits.

Keep in mind that superposition is based on linearity. For this reason, it is not applicable to the effect on power due to each source, because the power absorbed by a resistor depends on the square of the voltage or current. If the power value is needed, the current through (or voltage across) the element must be calculated first using superposition.

Example 4.3

Use the superposition theorem to find v in the circuit of Fig. 4.6.

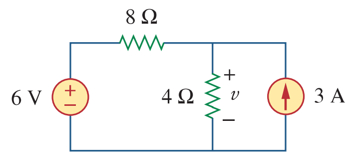

Figure 4.6
For Example 4.3.

Solution:
Since there are two sources, let

$$v = v_1 + v_2$$

where v_1 and v_2 are the contributions due to the 6-V voltage source and the 3-A current source, respectively. To obtain v_1, we set the current source to zero, as shown in Fig. 4.7(a). Applying KVL to the loop in Fig. 4.7(a) gives

$$12i_1 - 6 = 0 \quad \Rightarrow \quad i_1 = 0.5 \text{ A}$$

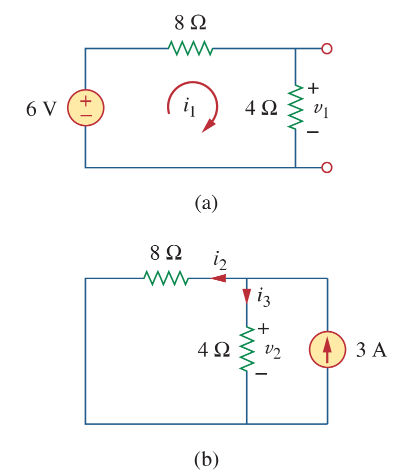

Figure 4.7
For Example 4.3: (a) calculating v_1, (b) calculating v_2.

Thus,

$$v_1 = 4i_1 = 2 \text{ V}$$

We may also use voltage division to get v_1 by writing

$$v_1 = \frac{4}{4+8}(6) = 2 \text{ V}$$

To get v_2, we set the voltage source to zero, as in Fig. 4.7(b). Using current division,

$$i_3 = \frac{8}{4+8}(3) = 2 \text{ A}$$

Hence,

$$v_2 = 4i_3 = 8 \text{ V}$$

And we find

$$v = v_1 + v_2 = 2 + 8 = 10 \text{ V}$$

Practice Problem 4.3

Using the superposition theorem, find v_o in the circuit of Fig. 4.8.

Answer: 7.4 V.

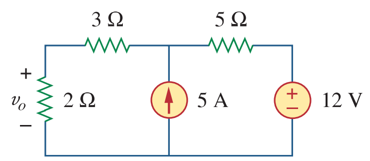

Figure 4.8
For Practice Prob. 4.3.

Example 4.4

Find i_o in the circuit of Fig. 4.9 using superposition.

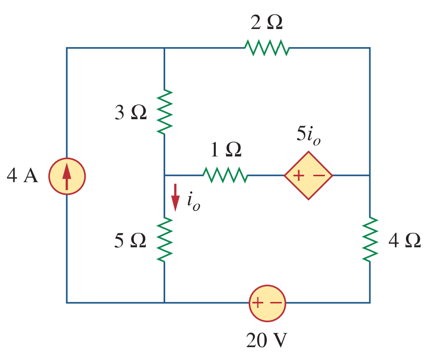

Figure 4.9
For Example 4.4.

Solution:
The circuit in Fig. 4.9 involves a dependent source, which must be left intact. We let

$$i_o = i'_o + i''_o \tag{4.4.1}$$

where i'_o and i''_o are due to the 4-A current source and 20-V voltage source respectively. To obtain i'_o, we turn off the 20-V source so that we have the circuit in Fig. 4.10(a). We apply mesh analysis in order to obtain i'_o. For loop 1,

$$i_1 = 4 \text{ A} \tag{4.4.2}$$

For loop 2,

$$-3i_1 + 6i_2 - 1i_3 - 5i'_o = 0 \tag{4.4.3}$$

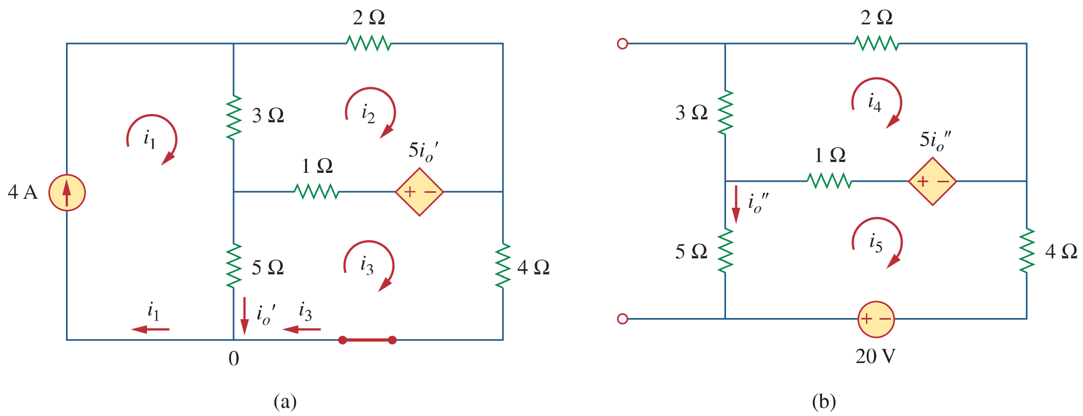

Figure 4.10
For Example 4.4: Applying superposition to (a) obtain i_o', (b) obtain i_o''.

For loop 3,

$$-5i_1 - 1i_2 + 10i_3 + 5i_o' = 0 \quad \textbf{(4.4.4)}$$

But at node 0,

$$i_3 = i_1 - i_o' = 4 - i_o' \quad \textbf{(4.4.5)}$$

Substituting Eqs. (4.4.2) and (4.4.5) into Eqs. (4.4.3) and (4.4.4) gives two simultaneous equations

$$3i_2 - 2i_o' = 8 \quad \textbf{(4.4.6)}$$

$$i_2 + 5i_o' = 20 \quad \textbf{(4.4.7)}$$

which can be solved to get

$$i_o' = \frac{52}{17}\text{ A} \quad \textbf{(4.4.8)}$$

To obtain i_o'', we turn off the 4-A current source so that the circuit becomes that shown in Fig. 4.10(b). For loop 4, KVL gives

$$6i_4 - i_5 - 5i_o'' = 0 \quad \textbf{(4.4.9)}$$

and for loop 5,

$$-i_4 + 10i_5 - 20 + 5i_o'' = 0 \quad \textbf{(4.4.10)}$$

But $i_5 = -i_o''$. Substituting this in Eqs. (4.4.9) and (4.4.10) gives

$$6i_4 - 4i_o'' = 0 \quad \textbf{(4.4.11)}$$

$$i_4 + 5i_o'' = -20 \quad \textbf{(4.4.12)}$$

which we solve to get

$$i_o'' = -\frac{60}{17}\text{ A} \quad \textbf{(4.4.13)}$$

Now substituting Eqs. (4.4.8) and (4.4.13) into Eq. (4.4.1) gives

$$i_o = -\frac{8}{17} = -0.4706\text{ A}$$

Practice Problem 4.4

Use superposition to find v_x in the circuit of Fig. 4.11.

Answer: $v_x = 31.25$ V.

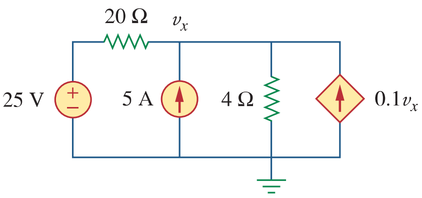

Figure 4.11
For Practice Prob. 4.4.

Example 4.5

For the circuit in Fig. 4.12, use the superposition theorem to find i.

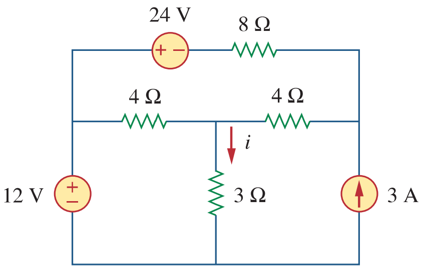

Figure 4.12
For Example 4.5.

Solution:
In this case, we have three sources. Let

$$i = i_1 + i_2 + i_3$$

where i_1, i_2, and i_3 are due to the 12-V, 24-V, and 3-A sources respectively. To get i_1, consider the circuit in Fig. 4.13(a). Combining 4 Ω (on the right-hand side) in series with 8 Ω gives 12 Ω. The 12 Ω in parallel with 4 Ω gives $12 \times 4/16 = 3$ Ω. Thus,

$$i_1 = \frac{12}{6} = 2 \text{ A}$$

To get i_2, consider the circuit in Fig. 4.13(b). Applying mesh analysis gives

$$16i_a - 4i_b + 24 = 0 \quad \Rightarrow \quad 4i_a - i_b = -6 \qquad \textbf{(4.5.1)}$$

$$7i_b - 4i_a = 0 \quad \Rightarrow \quad i_a = \frac{7}{4}i_b \qquad \textbf{(4.5.2)}$$

Substituting Eq. (4.5.2) into Eq. (4.5.1) gives

$$i_2 = i_b = -1$$

To get i_3, consider the circuit in Fig. 4.13(c). Using nodal analysis gives

$$3 = \frac{v_2}{8} + \frac{v_2 - v_1}{4} \quad \Rightarrow \quad 24 = 3v_2 - 2v_1 \qquad \textbf{(4.5.3)}$$

$$\frac{v_2 - v_1}{4} = \frac{v_1}{4} + \frac{v_1}{3} \quad \Rightarrow \quad v_2 = \frac{10}{3}v_1 \qquad \textbf{(4.5.4)}$$

Substituting Eq. (4.5.4) into Eq. (4.5.3) leads to $v_1 = 3$ and

$$i_3 = \frac{v_1}{3} = 1 \text{ A}$$

Thus,

$$i = i_1 + i_2 + i_3 = 2 - 1 + 1 = 2 \text{ A}$$

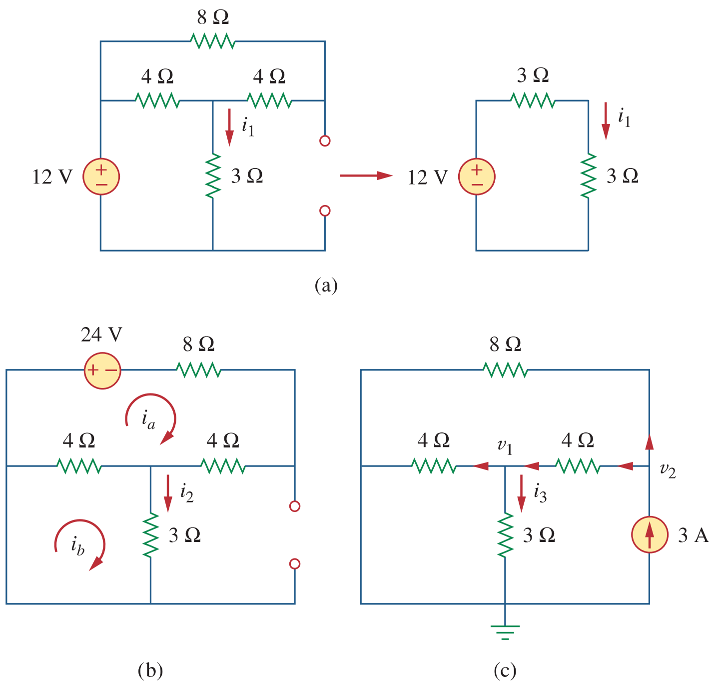

Figure 4.13
For Example 4.5.

Practice Problem 4.5

Find I in the circuit of Fig. 4.14 using the superposition principle.

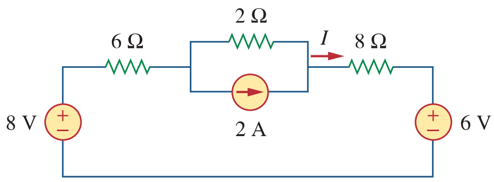

Figure 4.14
For Practice Prob. 4.5.

Answer: 375 mA.

4.4 Source Transformation

We have noticed that series-parallel combination and wye-delta transformation help simplify circuits. *Source transformation* is another tool for simplifying circuits. Basic to these tools is the concept of *equivalence*. We recall that an equivalent circuit is one whose v-i characteristics are identical with the original circuit.

In Section 3.6, we saw that node-voltage (or mesh-current) equations can be obtained by mere inspection of a circuit when the sources are all independent current (or all independent voltage) sources. It is therefore expedient in circuit analysis to be able to substitute a voltage source in series with a resistor for a current source in parallel with a resistor, or vice versa, as shown in Fig. 4.15. Either substitution is known as a *source transformation*.

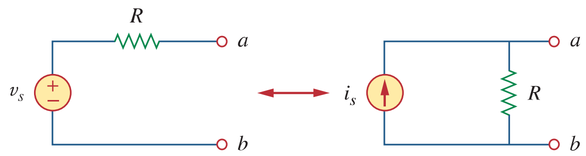

Figure 4.15
Transformation of independent sources.

> A **source transformation** is the process of replacing a voltage source v_s in series with a resistor R by a current source i_s in parallel with a resistor R, or vice versa.

The two circuits in Fig. 4.15 are equivalent—provided they have the same voltage-current relation at terminals *a-b*. It is easy to show that they are indeed equivalent. If the sources are turned off, the equivalent resistance at terminals *a-b* in both circuits is R. Also, when terminals *a-b* are short-circuited, the short-circuit current flowing from a to b is $i_{sc} = v_s/R$ in the circuit on the left-hand side and $i_{sc} = i_s$ for the circuit on the right-hand side. Thus, $v_s/R = i_s$ in order for the two circuits to be equivalent. Hence, source transformation requires that

$$v_s = i_s R \qquad \text{or} \qquad i_s = \frac{v_s}{R} \tag{4.5}$$

Source transformation also applies to dependent sources, provided we carefully handle the dependent variable. As shown in Fig. 4.16, a dependent voltage source in series with a resistor can be transformed to a dependent current source in parallel with the resistor or vice versa where we make sure that Eq. (4.5) is satisfied.

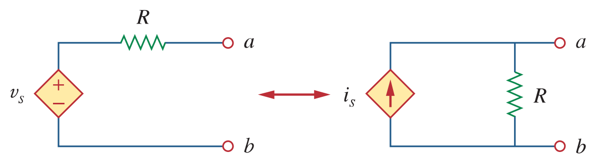

Figure 4.16
Transformation of dependent sources.

Like the wye-delta transformation we studied in Chapter 2, a source transformation does not affect the remaining part of the circuit. When applicable, source transformation is a powerful tool that allows circuit manipulations to ease circuit analysis. However, we should keep the following points in mind when dealing with source transformation.

1. Note from Fig. 4.15 (or Fig. 4.16) that the arrow of the current source is directed toward the positive terminal of the voltage source.
2. Note from Eq. (4.5) that source transformation is not possible when $R = 0$, which is the case with an ideal voltage source. However, for a practical, nonideal voltage source, $R \neq 0$. Similarly, an ideal current source with $R = \infty$ cannot be replaced by a finite voltage source. More will be said on ideal and nonideal sources in Section 4.10.1.

Example 4.6

Use source transformation to find v_o in the circuit of Fig. 4.17.

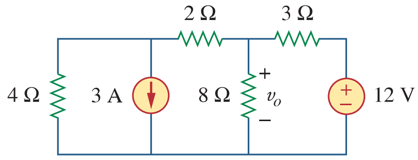

Figure 4.17
For Example 4.6.

Solution:
We first transform the current and voltage sources to obtain the circuit in Fig. 4.18(a). Combining the 4-Ω and 2-Ω resistors in series and transforming the 12-V voltage source gives us Fig. 4.18(b). We now combine the 3-Ω and 6-Ω resistors in parallel to get 2-Ω. We also combine the 2-A and 4-A current sources to get a 2-A source. Thus, by repeatedly applying source transformations, we obtain the circuit in Fig. 4.18(c).

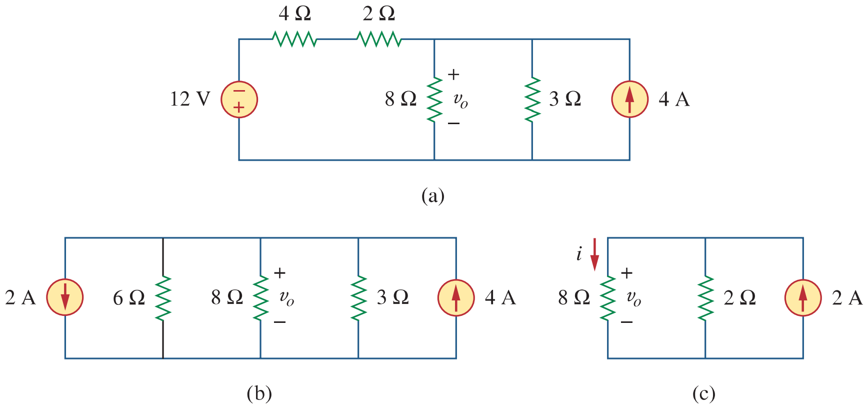

Figure 4.18
For Example 4.6.

We use current division in Fig. 4.18(c) to get

$$i = \frac{2}{2 + 8}(2) = 0.4 \text{ A}$$

and

$$v_o = 8i = 8(0.4) = 3.2 \text{ V}$$

Alternatively, since the 8-Ω and 2-Ω resistors in Fig. 4.18(c) are in parallel, they have the same voltage v_o across them. Hence,

$$v_o = (8 \parallel 2)(2 \text{ A}) = \frac{8 \times 2}{10}(2) = 3.2 \text{ V}$$

Practice Problem 4.6

Find i_o in the circuit of Fig. 4.19 using source transformation.

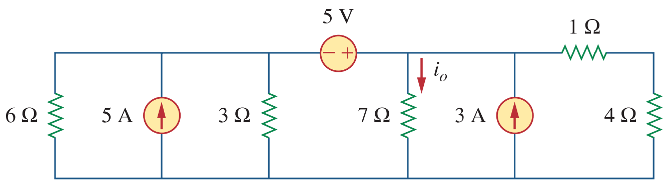

Figure 4.19
For Practice Prob. 4.6.

Answer: 1.78 A.

Example 4.7

Find v_x in Fig. 4.20 using source transformation.

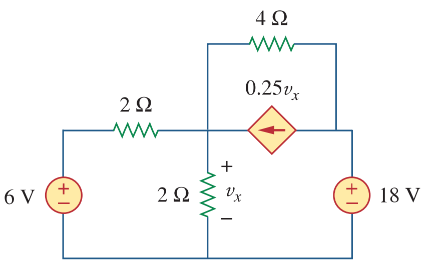

Figure 4.20
For Example 4.7.

Solution:

The circuit in Fig. 4.20 involves a voltage-controlled dependent current source. We transform this dependent current source as well as the 6-V independent voltage source as shown in Fig. 4.21(a). The 18-V voltage source is not transformed because it is not connected in series with any resistor. The two 2-Ω resistors in parallel combine to give a 1-Ω resistor, which is in parallel with the 3-A current source. The current source is transformed to a voltage source as shown in Fig. 4.21(b). Notice that the terminals for v_x are intact. Applying KVL around the loop in Fig. 4.21(b) gives

$$-3 + 5i + v_x + 18 = 0 \tag{4.7.1}$$

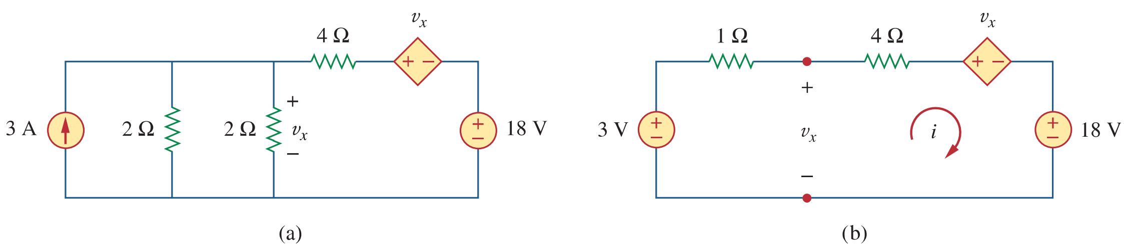

Figure 4.21
For Example 4.7: Applying source transformation to the circuit in Fig. 4.20.

Applying KVL to the loop containing only the 3-V voltage source, the 1-Ω resistor, and v_x yields

$$-3 + 1i + v_x = 0 \quad \Rightarrow \quad v_x = 3 - i \tag{4.7.2}$$

Substituting this into Eq. (4.7.1), we obtain

$$15 + 5i + 3 - i = 0 \quad \Rightarrow \quad i = -4.5 \text{ A}$$

Alternatively, we may apply KVL to the loop containing v_x, the 4-Ω resistor, the voltage-controlled dependent voltage source, and the 18-V voltage source in Fig. 4.21(b). We obtain

$$-v_x + 4i + v_x + 18 = 0 \quad \Rightarrow \quad i = -4.5 \text{ A}$$

Thus, $v_x = 3 - i = 7.5$ V.

Practice Problem 4.7

Use source transformation to find i_x in the circuit shown in Fig. 4.22.

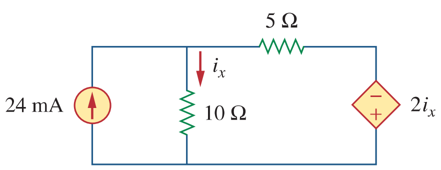

Figure 4.22
For Practice Prob. 4.7.

Answer: 7.059 mA.

4.5 Thevenin's Theorem

It often occurs in practice that a particular element in a circuit is variable (usually called the *load*) while other elements are fixed. As a typical example, a household outlet terminal may be connected to different appliances constituting a variable load. Each time the variable element is changed, the entire circuit has to be analyzed all over again. To avoid this problem, Thevenin's theorem provides a technique by which the fixed part of the circuit is replaced by an equivalent circuit.

According to Thevenin's theorem, the linear circuit in Fig. 4.23(a) can be replaced by that in Fig. 4.23(b). (The load in Fig. 4.23 may be a single resistor or another circuit.) The circuit to the left of the terminals *a-b* in Fig. 4.23(b) is known as the *Thevenin equivalent circuit*; it was developed in 1883 by M. Leon Thevenin (1857–1926), a French telegraph engineer.

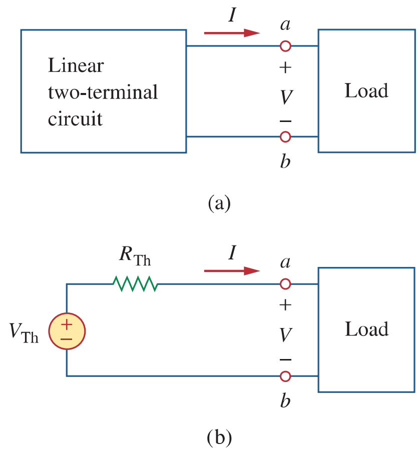

Figure 4.23
Replacing a linear two-terminal circuit by its Thevenin equivalent: (a) original circuit, (b) the Thevenin equivalent circuit.

> **Thevenin's theorem** states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a voltage source V_{Th} in series with a resistor R_{Th}, where V_{Th} is the open-circuit voltage at the terminals and R_{Th} is the input or equivalent resistance at the terminals when the independent sources are turned off.

The proof of the theorem will be given later, in Section 4.7. Our major concern right now is how to find the Thevenin equivalent voltage V_{Th} and resistance R_{Th}. To do so, suppose the two circuits in Fig. 4.23 are equivalent. Two circuits are said to be *equivalent* if they have the same voltage-current relation at their terminals. Let us find out what will make the two circuits in Fig. 4.23 equivalent. If the terminals *a-b* are made open-circuited (by removing the load), no current flows, so that the open-circuit voltage across the terminals *a-b* in Fig. 4.23(a) must be equal to the voltage source V_{Th} in Fig. 4.23(b), since the two circuits are equivalent. Thus V_{Th} is the open-circuit voltage across the terminals as shown in Fig. 4.24(a); that is,

$$V_{Th} = v_{oc} \quad (4.6)$$

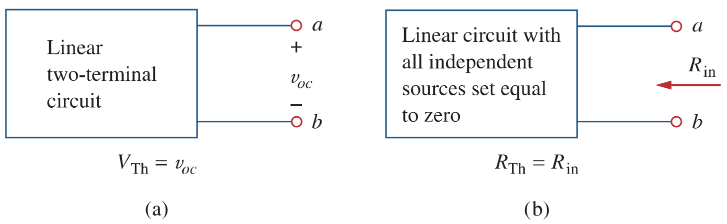

Figure 4.24
Finding V_{Th} and R_{Th}.

Again, with the load disconnected and terminals *a-b* open-circuited, we turn off all independent sources. The input resistance (or equivalent resistance) of the dead circuit at the terminals *a-b* in Fig. 4.23(a) must be equal to R_{Th} in Fig. 4.23(b) because the two circuits are equivalent. Thus, R_{Th} is the input resistance at the terminals when the independent sources are turned off, as shown in Fig. 4.24(b); that is,

$$R_{Th} = R_{in} \quad (4.7)$$

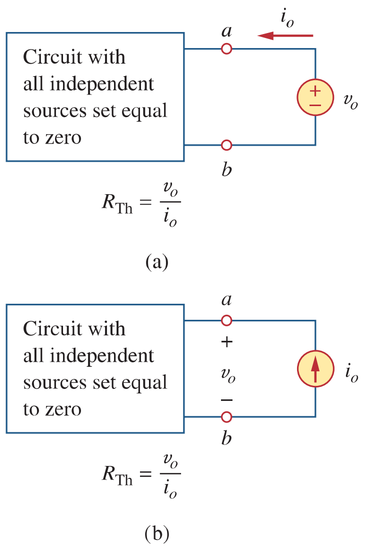

Figure 4.25
Finding R_{Th} when circuit has dependent sources.

Later we will see that an alternative way of finding R_{Th} is $R_{Th} = v_{oc}/i_{sc}$.

To apply this idea in finding the Thevenin resistance R_{Th}, we need to consider two cases.

CASE 1 If the network has no dependent sources, we turn off all independent sources. R_{Th} is the input resistance of the network looking between terminals a and b, as shown in Fig. 4.24(b).

CASE 2 If the network has dependent sources, we turn off all independent sources. As with superposition, dependent sources are not to be turned off because they are controlled by circuit variables. We apply a voltage source v_o at terminals a and b and determine the resulting current i_o. Then $R_{Th} = v_o/i_o$, as shown in Fig. 4.25(a). Alternatively, we may insert a current source i_o at terminals a-b as shown in Fig. 4.25(b) and find the terminal voltage v_o. Again $R_{Th} = v_o/i_o$. Either of the two approaches will give the same result. In either approach we may assume any value of v_o and i_o. For example, we may use $v_o = 1$ V or $i_o = 1$ A, or even use unspecified values of v_o or i_o.

It often occurs that R_{Th} takes a negative value. In this case, the negative resistance ($v = -iR$) implies that the circuit is supplying power. This is possible in a circuit with dependent sources; Example 4.10 will illustrate this.

Thevenin's theorem is very important in circuit analysis. It helps simplify a circuit. A large circuit may be replaced by a single independent voltage source and a single resistor. This replacement technique is a powerful tool in circuit design.

As mentioned earlier, a linear circuit with a variable load can be replaced by the Thevenin equivalent, exclusive of the load. The equivalent network behaves the same way externally as the original circuit. Consider a linear circuit terminated by a load R_L, as shown in Fig. 4.26(a). The current I_L through the load and the voltage V_L across the load are easily determined once the Thevenin equivalent of the circuit at the load's terminals is obtained, as shown in Fig. 4.26(b). From Fig. 4.26(b), we obtain

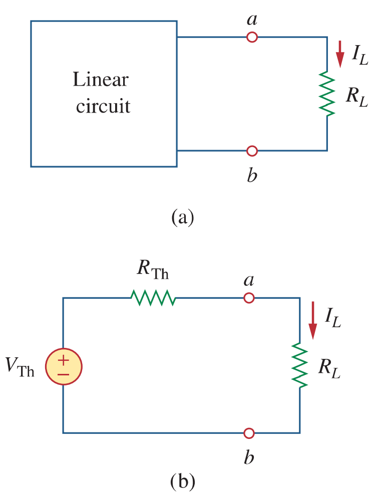

Figure 4.26
A circuit with a load: (a) original circuit, (b) Thevenin equivalent.

$$I_L = \frac{V_{Th}}{R_{Th} + R_L} \tag{4.8a}$$

$$V_L = R_L I_L = \frac{R_L}{R_{Th} + R_L} V_{Th} \tag{4.8b}$$

Note from Fig. 4.26(b) that the Thevenin equivalent is a simple voltage divider, yielding V_L by mere inspection.

Example 4.8

Find the Thevenin equivalent circuit of the circuit shown in Fig. 4.27, to the left of the terminals a-b. Then find the current through $R_L = 6$, 16, and 36 Ω.

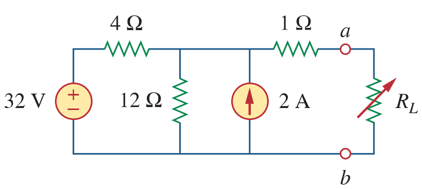

Figure 4.27
For Example 4.8.

Solution:
We find R_{Th} by turning off the 32-V voltage source (replacing it with a short circuit) and the 2-A current source (replacing it with an

open circuit). The circuit becomes what is shown in Fig. 4.28(a). Thus,

$$R_{Th} = 4 \parallel 12 + 1 = \frac{4 \times 12}{16} + 1 = 4\ \Omega$$

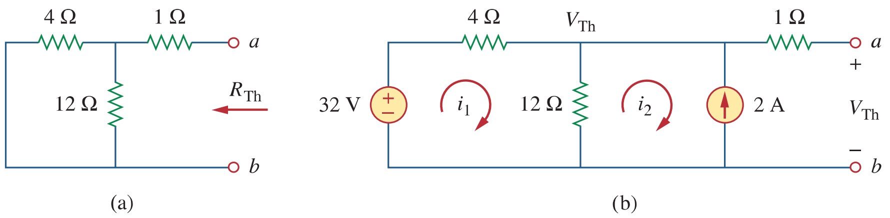

Figure 4.28
For Example 4.8: (a) finding R_{Th}, (b) finding V_{Th}.

To find V_{Th}, consider the circuit in Fig. 4.28(b). Applying mesh analysis to the two loops, we obtain

$$-32 + 4i_1 + 12(i_1 - i_2) = 0, \qquad i_2 = -2\text{ A}$$

Solving for i_1, we get $i_1 = 0.5$ A. Thus,

$$V_{Th} = 12(i_1 - i_2) = 12(0.5 + 2.0) = 30\text{ V}$$

Alternatively, it is even easier to use nodal analysis. We ignore the 1-Ω resistor since no current flows through it. At the top node, KCL gives

$$\frac{32 - V_{Th}}{4} + 2 = \frac{V_{Th}}{12}$$

or

$$96 - 3V_{Th} + 24 = V_{Th} \quad \Rightarrow \quad V_{Th} = 30\text{ V}$$

as obtained before. We could also use source transformation to find V_{Th}.

The Thevenin equivalent is shown in Fig. 4.29. The current through R_L is

$$I_L = \frac{V_{Th}}{R_{Th} + R_L} = \frac{30}{4 + R_L}$$

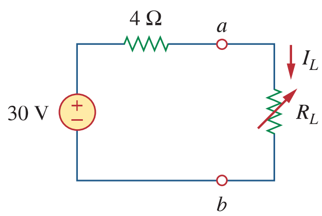

Figure 4.29
The Thevenin equivalent circuit for Example 4.8.

When $R_L = 6$,

$$I_L = \frac{30}{10} = 3\text{ A}$$

When $R_L = 16$,

$$I_L = \frac{30}{20} = 1.5\text{ A}$$

When $R_L = 36$,

$$I_L = \frac{30}{40} = 0.75\text{ A}$$

Practice Problem 4.8

Using Thevenin's theorem, find the equivalent circuit to the left of the terminals in the circuit of Fig. 4.30. Then find I.

Answer: $V_{Th} = 6$ V, $R_{Th} = 3\ \Omega$, $I = 1.5$ A.

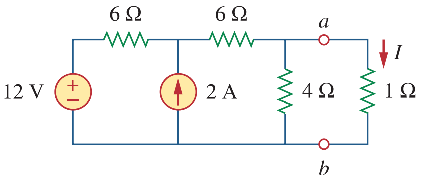

Figure 4.30
For Practice Prob. 4.8.

Example 4.9

Find the Thevenin equivalent of the circuit in Fig. 4.31 at terminals *a-b*.

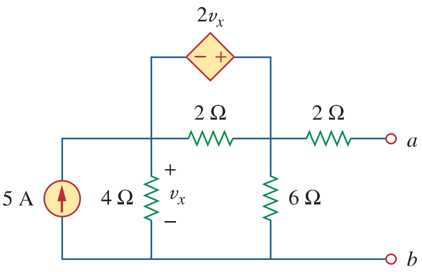

Figure 4.31
For Example 4.9.

Solution:
This circuit contains a dependent source, unlike the circuit in the previous example. To find R_{Th}, we set the independent source equal to zero but leave the dependent source alone. Because of the presence of the dependent source, however, we excite the network with a voltage source v_o connected to the terminals as indicated in Fig. 4.32(a). We may set $v_o = 1$ V to ease calculation, since the circuit is linear. Our goal is to find the current i_o through the terminals, and then obtain $R_{Th} = 1/i_o$. (Alternatively, we may insert a 1-A current source, find the corresponding voltage v_o, and obtain $R_{Th} = v_o/1$.)

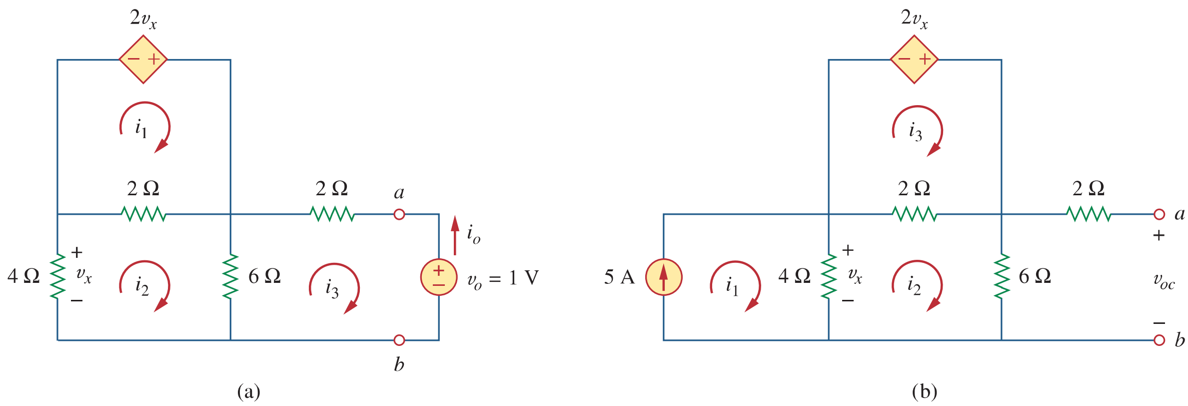

Figure 4.32
Finding R_{Th} and V_{Th} for Example 4.9.

Applying mesh analysis to loop 1 in the circuit of Fig. 4.32(a) results in

$$-2v_x + 2(i_1 - i_2) = 0 \qquad \text{or} \qquad v_x = i_1 - i_2$$

But $-4i_2 = v_x = i_1 - i_2$; hence,

$$i_1 = -3i_2 \tag{4.9.1}$$

For loops 2 and 3, applying KVL produces

$$4i_2 + 2(i_2 - i_1) + 6(i_2 - i_3) = 0 \tag{4.9.2}$$

$$6(i_3 - i_2) + 2i_3 + 1 = 0 \tag{4.9.3}$$

Solving these equations gives

$$i_3 = -\frac{1}{6}\text{ A}$$

But $i_o = -i_3 = 1/6$ A. Hence,

$$R_{\text{Th}} = \frac{1\text{ V}}{i_o} = 6\ \Omega$$

To get V_{Th}, we find v_{oc} in the circuit of Fig. 4.32(b). Applying mesh analysis, we get

$$i_1 = 5 \tag{4.9.4}$$

$$-2v_x + 2(i_3 - i_2) = 0 \quad \Rightarrow \quad v_x = i_3 - i_2 \tag{4.9.5}$$

$$4(i_2 - i_1) + 2(i_2 - i_3) + 6i_2 = 0$$

or

$$12i_2 - 4i_1 - 2i_3 = 0 \tag{4.9.6}$$

But $4(i_1 - i_2) = v_x$. Solving these equations leads to $i_2 = 10/3$. Hence,

$$V_{\text{Th}} = v_{oc} = 6i_2 = 20\text{ V}$$

The Thevenin equivalent is as shown in Fig. 4.33.

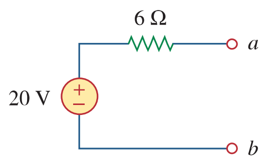

Figure 4.33
The Thevenin equivalent of the circuit in Fig. 4.31.

Practice Problem 4.9

Find the Thevenin equivalent circuit of the circuit in Fig. 4.34 to the left of the terminals.

Answer: $V_{\text{Th}} = 5.333$ V, $R_{\text{Th}} = 444.4$ mΩ.

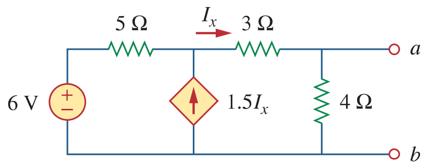

Figure 4.34
For Practice Prob. 4.9.

Example 4.10

Determine the Thevenin equivalent of the circuit in Fig. 4.35(a) at terminals *a*-*b*.

Solution:

1. **Define.** The problem is clearly defined; we are to determine the Thevenin equivalent of the circuit shown in Fig. 4.35(a).
2. **Present.** The circuit contains a 2-Ω resistor in parallel with a 4-Ω resistor. These are, in turn, in parallel with a dependent current source. It is important to note that there are no independent sources.
3. **Alternative.** The first thing to consider is that, since we have no independent sources in this circuit, we must excite the circuit externally. In addition, when you have no independent sources you will not have a value for V_{Th}; you will only have to find R_{Th}.

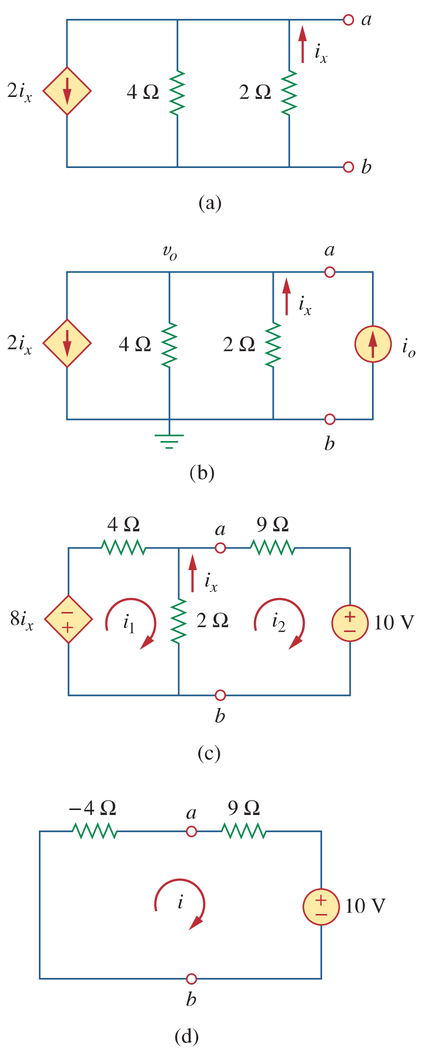

Figure 4.35
For Example 4.10.

The simplest approach is to excite the circuit with either a 1-V voltage source or a 1-A current source. Since we will end up with an equivalent resistance (either positive or negative), I prefer to use the current source and nodal analysis which will yield a voltage at the output terminals equal to the resistance (with 1 A flowing in, v_o is equal to 1 times the equivalent resistance).

As an alternative, the circuit could also be excited by a 1-V voltage source and mesh analysis could be used to find the equivalent resistance.

4. **Attempt.** We start by writing the nodal equation at a in Fig. 4.35(b) assuming $i_o = 1$ A.

$$2i_x + (v_o - 0)/4 + (v_o - 0)/2 + (-1) = 0 \qquad \textbf{(4.10.1)}$$

Since we have two unknowns and only one equation, we will need a constraint equation.

$$i_x = (0 - v_o)/2 = -v_o/2 \qquad \textbf{(4.10.2)}$$

Substituting Eq. (4.10.2) into Eq. (4.10.1) yields

$$2(-v_o/2) + (v_o - 0)/4 + (v_o - 0)/2 + (-1) = 0$$
$$= (-1 + \tfrac{1}{4} + \tfrac{1}{2})v_o - 1 \qquad \text{or} \qquad v_o = -4\text{ V}$$

Since $v_o = 1 \times R_{\text{Th}}$, then $R_{\text{Th}} = v_o/1 = \mathbf{-4\ \Omega}$.

The negative value of the resistance tells us that, according to the passive sign convention, the circuit in Fig. 4.35(a) is supplying power. Of course, the resistors in Fig. 4.35(a) cannot supply power (they absorb power); it is the dependent source that supplies the power. This is an example of how a dependent source and resistors could be used to simulate negative resistance.

5. **Evaluate.** First of all, we note that the answer has a negative value. We know this is not possible in a passive circuit, but in this circuit we do have an active device (the dependent current source). Thus, the equivalent circuit is essentially an active circuit that can supply power.

Now we must evaluate the solution. The best way to do this is to perform a check, using a different approach, and see if we obtain the same solution. Let us try connecting a 9-Ω resistor in series with a 10-V voltage source across the output terminals of the original circuit and then the Thevenin equivalent. To make the circuit easier to solve, we can take and change the parallel current source and 4-Ω resistor to a series voltage source and 4-Ω resistor by using source transformation. This, with the new load, gives us the circuit shown in Fig. 4.35(c).

We can now write two mesh equations.

$$8i_x + 4i_1 + 2(i_1 - i_2) = 0$$
$$2(i_2 - i_1) + 9i_2 + 10 = 0$$

Note, we only have two equations but have 3 unknowns, so we need a constraint equation. We can use

$$i_x = i_2 - i_1$$

This leads to a new equation for loop 1. Simplifying leads to

$$(4 + 2 - 8)i_1 + (-2 + 8)i_2 = 0$$

or

$$-2i_1 + 6i_2 = 0 \qquad \text{or} \qquad i_1 = 3i_2$$
$$-2i_1 + 11i_2 = -10$$

Substituting the first equation into the second gives

$$-6i_2 + 11i_2 = -10 \qquad \text{or} \qquad i_2 = -10/5 = \mathbf{-2\ A}$$

Using the Thevenin equivalent is quite easy since we have only one loop, as shown in Fig. 4.35(d).

$$-4i + 9i + 10 = 0 \qquad \text{or} \qquad i = -10/5 = \mathbf{-2\ A}$$

6. **Satisfactory?** Clearly we have found the value of the equivalent circuit as required by the problem statement. Checking does validate that solution (we compared the answer we obtained by using the equivalent circuit with one obtained by using the load with the original circuit). We can present all this as a solution to the problem.

Practice Problem 4.10

Obtain the Thevenin equivalent of the circuit in Fig. 4.36.

Answer: $V_{Th} = 0$ V, $R_{Th} = -7.5\ \Omega$.

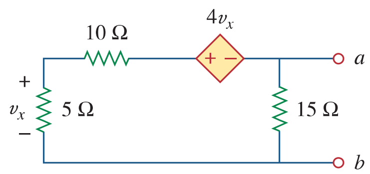

Figure 4.36
For Practice Prob. 4.10.

4.6 Norton's Theorem

In 1926, about 43 years after Thevenin published his theorem, E. L. Norton, an American engineer at Bell Telephone Laboratories, proposed a similar theorem.

> **Norton's theorem** states that a linear two-terminal circuit can be replaced by an equivalent circuit consisting of a current source I_N in parallel with a resistor R_N, where I_N is the short-circuit current through the terminals and R_N is the input or equivalent resistance at the terminals when the independent sources are turned off.

Thus, the circuit in Fig. 4.37(a) can be replaced by the one in Fig. 4.37(b).

The proof of Norton's theorem will be given in the next section. For now, we are mainly concerned with how to get R_N and I_N. We find R_N in the same way we find R_{Th}. In fact, from what we know about source transformation, the Thevenin and Norton resistances are equal; that is,

$$R_N = R_{Th} \tag{4.9}$$

To find the Norton current I_N, we determine the short-circuit current flowing from terminal a to b in both circuits in Fig. 4.37. It is evident

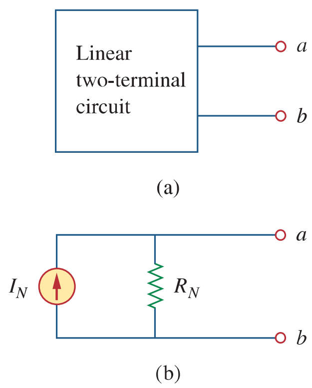

Figure 4.37
(a) Original circuit, (b) Norton equivalent circuit.

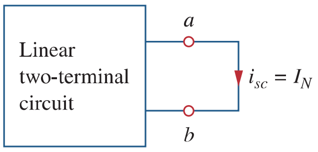

Figure 4.38
Finding Norton current I_N.

that the short-circuit current in Fig. 4.37(b) is I_N. This must be the same short-circuit current from terminal a to b in Fig. 4.37(a), since the two circuits are equivalent. Thus,

$$I_N = i_{sc} \tag{4.10}$$

shown in Fig. 4.38. Dependent and independent sources are treated the same way as in Thevenin's theorem.

Observe the close relationship between Norton's and Thevenin's theorems: $R_N = R_{\text{Th}}$ as in Eq. (4.9), and

$$I_N = \frac{V_{\text{Th}}}{R_{\text{Th}}} \tag{4.11}$$

The Thevenin and Norton equivalent circuits are related by a source transformation.

This is essentially source transformation. For this reason, source transformation is often called Thevenin-Norton transformation.

Since V_{Th}, I_N, and R_{Th} are related according to Eq. (4.11), to determine the Thevenin or Norton equivalent circuit requires that we find:

- The open-circuit voltage v_{oc} across terminals a and b.
- The short-circuit current i_{sc} at terminals a and b.
- The equivalent or input resistance R_{in} at terminals a and b when all independent sources are turned off.

We can calculate any two of the three using the method that takes the least effort and use them to get the third using Ohm's law. Example 4.11 will illustrate this. Also, since

$$V_{\text{Th}} = v_{oc} \tag{4.12a}$$

$$I_N = i_{sc} \tag{4.12b}$$

$$R_{\text{Th}} = \frac{v_{oc}}{i_{sc}} = R_N \tag{4.12c}$$

the open-circuit and short-circuit tests are sufficient to find any Thevenin or Norton equivalent, of a circuit which contains at least one independent source.

Example 4.11

Find the Norton equivalent circuit of the circuit in Fig. 4.39 at terminals a-b.

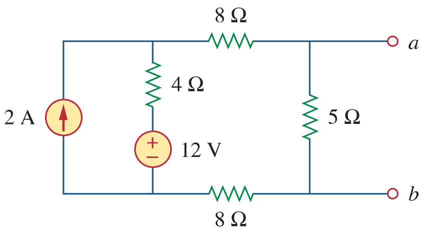

Figure 4.39
For Example 4.11.

Solution:
We find R_N in the same way we find R_{Th} in the Thevenin equivalent circuit. Set the independent sources equal to zero. This leads to the circuit in Fig. 4.40(a), from which we find R_N. Thus,

$$R_N = 5 \parallel (8 + 4 + 8) = 5 \parallel 20 = \frac{20 \times 5}{25} = 4\ \Omega$$

To find I_N, we short-circuit terminals a and b, as shown in Fig. 4.40(b). We ignore the 5-Ω resistor because it has been short-circuited. Applying mesh analysis, we obtain

$$i_1 = 2\text{ A}, \qquad 20i_2 - 4i_1 - 12 = 0$$

From these equations, we obtain

$$i_2 = 1\text{ A} = i_{sc} = I_N$$

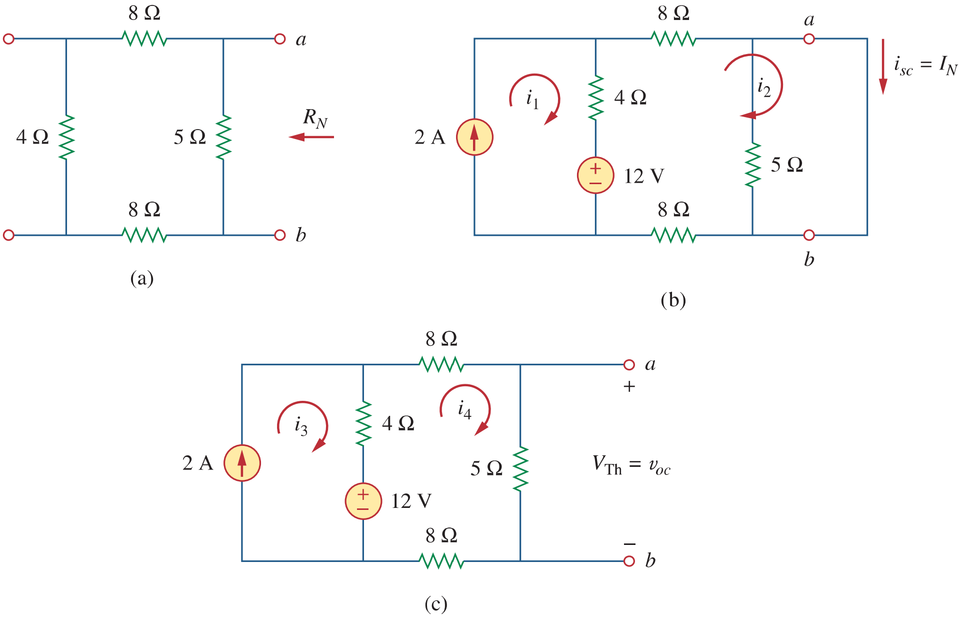

Figure 4.40
For Example 4.11; finding: (a) R_N, (b) $I_N = i_{sc}$, (c) $V_{Th} = v_{oc}$.

Alternatively, we may determine I_N from V_{Th}/R_{Th}. We obtain V_{Th} as the open-circuit voltage across terminals a and b in Fig. 4.40(c). Using mesh analysis, we obtain

$$i_3 = 2 \text{ A}$$

$$25i_4 - 4i_3 - 12 = 0 \quad \Rightarrow \quad i_4 = 0.8 \text{ A}$$

and

$$v_{oc} = V_{Th} = 5i_4 = 4 \text{ V}$$

Hence,

$$I_N = \frac{V_{Th}}{R_{Th}} = \frac{4}{4} = 1 \text{ A}$$

as obtained previously. This also serves to confirm Eq. (4.12c) that $R_{Th} = v_{oc}/i_{sc} = 4/1 = 4\ \Omega$. Thus, the Norton equivalent circuit is as shown in Fig. 4.41.

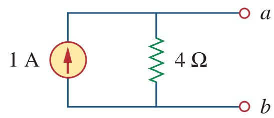

Figure 4.41
Norton equivalent of the circuit in Fig. 4.39.

Practice Problem 4.11

Find the Norton equivalent circuit for the circuit in Fig. 4.42, at terminals a-b.

Answer: $R_N = 3\ \Omega$, $I_N = 4.5$ A.

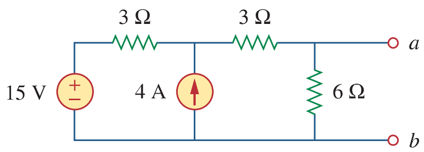

Figure 4.42
For Practice Prob. 4.11.

Example 4.12

Using Norton's theorem, find R_N and I_N of the circuit in Fig. 4.43 at terminals *a*-*b*.

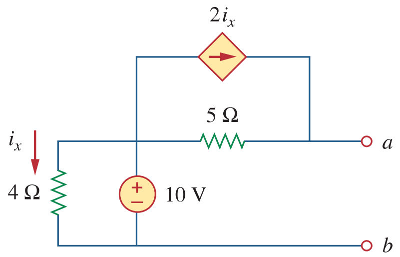

Figure 4.43
For Example 4.12.

Solution:
To find R_N, we set the independent voltage source equal to zero and connect a voltage source of $v_o = 1$ V (or any unspecified voltage v_o) to the terminals. We obtain the circuit in Fig. 4.44(a). We ignore the 4-Ω resistor because it is short-circuited. Also due to the short circuit, the 5-Ω resistor, the voltage source, and the dependent current source are all in parallel. Hence, $i_x = 0$. At node *a*, $i_o = \frac{1v}{5\Omega} = 0.2$ A, and

$$R_N = \frac{v_o}{i_o} = \frac{1}{0.2} = 5\ \Omega$$

To find I_N, we short-circuit terminals *a* and *b* and find the current i_{sc}, as indicated in Fig. 4.44(b). Note from this figure that the 4-Ω resistor, the 10-V voltage source, the 5-Ω resistor, and the dependent current source are all in parallel. Hence,

$$i_x = \frac{10}{4} = 2.5\ \text{A}$$

At node *a*, KCL gives

$$i_{sc} = \frac{10}{5} + 2i_x = 2 + 2(2.5) = 7\ \text{A}$$

Thus,

$$I_N = 7\ \text{A}$$

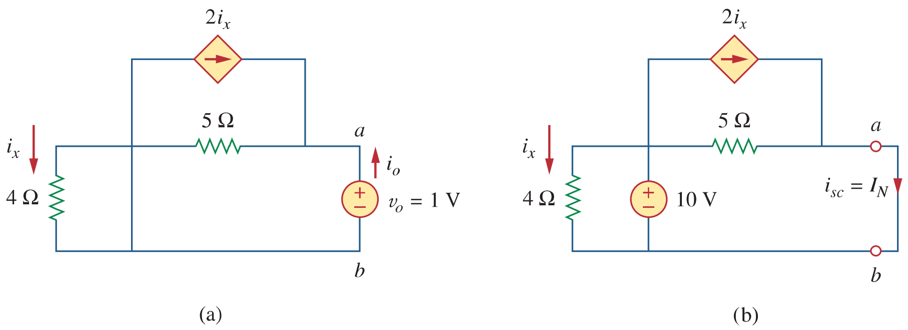

Figure 4.44
For Example 4.12: (a) finding R_N, (b) finding I_N.

Practice Problem 4.12

Find the Norton equivalent circuit of the circuit in Fig. 4.45 at terminals *a*-*b*.

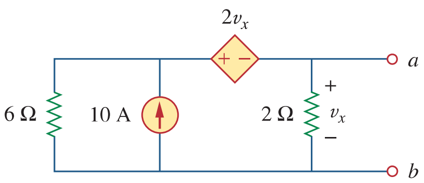

Figure 4.45
For Practice Prob. 4.12.

Answer: $R_N = 1\ \Omega$, $I_N = 10$ A.

4.7 † Derivations of Thevenin's and Norton's Theorems

In this section, we will prove Thevenin's and Norton's theorems using the superposition principle.

Consider the linear circuit in Fig. 4.46(a). It is assumed that the circuit contains resistors and dependent and independent sources. We have access to the circuit via terminals a and b, through which current from an external source is applied. Our objective is to ensure that the voltage-current relation at terminals a and b is identical to that of the Thevenin equivalent in Fig. 4.46(b). For the sake of simplicity, suppose the linear circuit in Fig. 4.46(a) contains two independent voltage sources v_{s1} and v_{s2} and two independent current sources i_{s1} and i_{s2}. We may obtain any circuit variable, such as the terminal voltage v, by applying superposition. That is, we consider the contribution due to each independent source including the external source i. By superposition, the terminal voltage v is

$$v = A_0 i + A_1 v_{s1} + A_2 v_{s2} + A_3 i_{s1} + A_4 i_{s2} \tag{4.13}$$

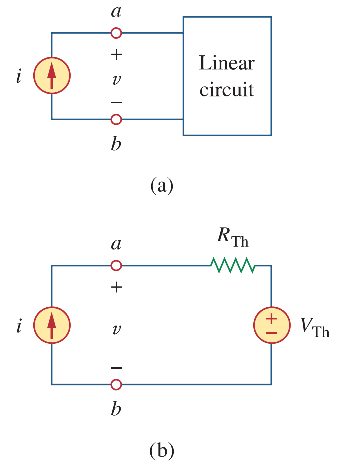

Figure 4.46
Derivation of Thevenin equivalent: (a) a current-driven circuit, (b) its Thevenin equivalent.

where A_0, A_1, A_2, A_3, and A_4 are constants. Each term on the right-hand side of Eq. (4.13) is the contribution of the related independent source; that is, $A_0 i$ is the contribution to v due to the external current source i, $A_1 v_{s1}$ is the contribution due to the voltage source v_{s1}, and so on. We may collect terms for the internal independent sources together as B_0, so that Eq. (4.13) becomes

$$v = A_0 i + B_0 \tag{4.14}$$

where $B_0 = A_1 v_{s1} + A_2 v_{s2} + A_3 i_{s1} + A_4 i_{s2}$. We now want to evaluate the values of constants A_0 and B_0. When the terminals a and b are open-circuited, $i = 0$ and $v = B_0$. Thus, B_0 is the open-circuit voltage v_{oc}, which is the same as V_{Th}, so

$$B_0 = V_{\text{Th}} \tag{4.15}$$

When all the internal sources are turned off, $B_0 = 0$. The circuit can then be replaced by an equivalent resistance R_{eq}, which is the same as R_{Th}, and Eq. (4.14) becomes

$$v = A_0 i = R_{\text{Th}} i \quad \Rightarrow \quad A_0 = R_{\text{Th}} \tag{4.16}$$

Substituting the values of A_0 and B_0 in Eq. (4.14) gives

$$v = R_{\text{Th}} i + V_{\text{Th}} \tag{4.17}$$

which expresses the voltage-current relation at terminals a and b of the circuit in Fig. 4.46(b). Thus, the two circuits in Fig. 4.46(a) and 4.46(b) are equivalent.

When the same linear circuit is driven by a voltage source v as shown in Fig. 4.47(a), the current flowing into the circuit can be obtained by superposition as

$$i = C_0 v + D_0 \tag{4.18}$$

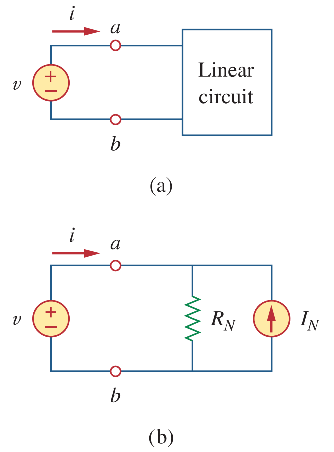

Figure 4.47
Derivation of Norton equivalent: (a) a voltage-driven circuit, (b) its Norton equivalent.

where $C_0 v$ is the contribution to i due to the external voltage source v and D_0 contains the contributions to i due to all internal independent sources. When the terminals a-b are short-circuited, $v = 0$ so that

$i = D_0 = -i_{sc}$, where i_{sc} is the short-circuit current flowing out of terminal a, which is the same as the Norton current I_N, i.e.,

$$D_0 = -I_N \tag{4.19}$$

When all the internal independent sources are turned off, $D_0 = 0$ and the circuit can be replaced by an equivalent resistance R_{eq} (or an equivalent conductance $G_{eq} = 1/R_{eq}$), which is the same as R_{Th} or R_N. Thus Eq. (4.19) becomes

$$i = \frac{v}{R_{Th}} - I_N \tag{4.20}$$

This expresses the voltage-current relation at terminals a-b of the circuit in Fig. 4.47(b), confirming that the two circuits in Fig. 4.47(a) and 4.47(b) are equivalent.

4.8 Maximum Power Transfer

In many practical situations, a circuit is designed to provide power to a load. There are applications in areas such as communications where it is desirable to maximize the power delivered to a load. We now address the problem of delivering the maximum power to a load when given a system with known internal losses. It should be noted that this will result in significant internal losses greater than or equal to the power delivered to the load.

The Thevenin equivalent is useful in finding the maximum power a linear circuit can deliver to a load. We assume that we can adjust the load resistance R_L. If the entire circuit is replaced by its Thevenin equivalent except for the load, as shown in Fig. 4.48, the power delivered to the load is

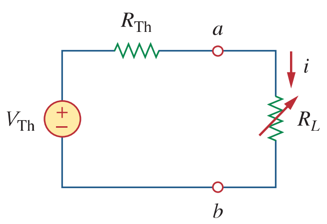

Figure 4.48
The circuit used for maximum power transfer.

$$p = i^2 R_L = \left(\frac{V_{Th}}{R_{Th} + R_L}\right)^2 R_L \tag{4.21}$$

For a given circuit, V_{Th} and R_{Th} are fixed. By varying the load resistance R_L, the power delivered to the load varies as sketched in Fig. 4.49. We notice from Fig. 4.49 that the power is small for small or large values of R_L but maximum for some value of R_L between 0 and ∞. We now want to show that this maximum power occurs when R_L is equal to R_{Th}. This is known as the *maximum power theorem.*

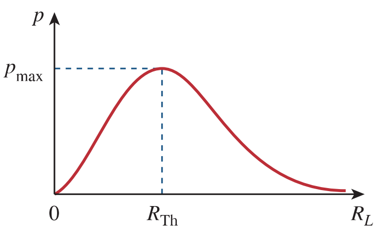

Figure 4.49
Power delivered to the load as a function of R_L.

> **Maximum power** is transferred to the load when the load resistance equals the Thevenin resistance as seen from the load ($R_L = R_{Th}$).

To prove the maximum power transfer theorem, we differentiate p in Eq. (4.21) with respect to R_L and set the result equal to zero. We obtain

$$\frac{dp}{dR_L} = V_{Th}^2 \left[\frac{(R_{Th} + R_L)^2 - 2R_L(R_{Th} + R_L)}{(R_{Th} + R_L)^4}\right]$$
$$= V_{Th}^2 \left[\frac{(R_{Th} + R_L - 2R_L)}{(R_{Th} + R_L)^3}\right] = 0$$

This implies that

$$0 = (R_{Th} + R_L - 2R_L) = (R_{Th} - R_L) \quad (4.22)$$

which yields

$$R_L = R_{Th} \quad (4.23)$$

showing that the maximum power transfer takes place when the load resistance R_L equals the Thevenin resistance R_{Th}. We can readily confirm that Eq. (4.23) gives the maximum power by showing that $d^2p/dR_L^2 < 0$.

The source and load are said to be *matched* when $R_L = R_{Th}$.

The maximum power transferred is obtained by substituting Eq. (4.23) into Eq. (4.21), for

$$p_{max} = \frac{V_{Th}^2}{4R_{Th}} \quad (4.24)$$

Equation (4.24) applies only when $R_L = R_{Th}$. When $R_L \neq R_{Th}$, we compute the power delivered to the load using Eq. (4.21).

Example 4.13

Find the value of R_L for maximum power transfer in the circuit of Fig. 4.50. Find the maximum power.

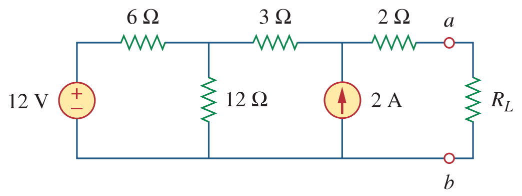

Figure 4.50
For Example 4.13.

Solution:
We need to find the Thevenin resistance R_{Th} and the Thevenin voltage V_{Th} across the terminals *a-b*. To get R_{Th}, we use the circuit in Fig. 4.51(a) and obtain

$$R_{Th} = 2 + 3 + 6 \| 12 = 5 + \frac{6 \times 12}{18} = 9\ \Omega$$

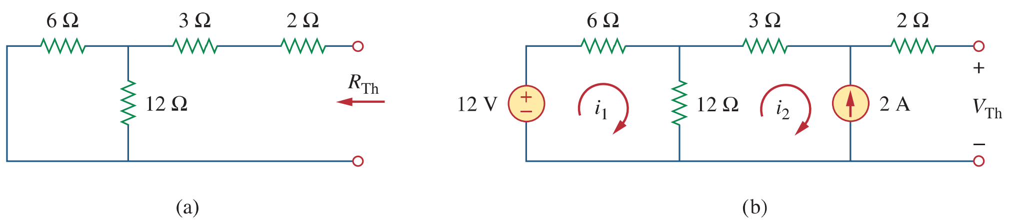

Figure 4.51
For Example 4.13: (a) finding R_{Th}, (b) finding V_{Th}.

To get V_{Th}, we consider the circuit in Fig. 4.51(b). Applying mesh analysis gives

$$-12 + 18i_1 - 12i_2 = 0, \qquad i_2 = -2 \text{ A}$$

Solving for i_1, we get $i_1 = -2/3$. Applying KVL around the outer loop to get V_{Th} across terminals *a-b*, we obtain

$$-12 + 6i_1 + 3i_2 + 2(0) + V_{Th} = 0 \qquad \Rightarrow \qquad V_{Th} = 22 \text{ V}$$

For maximum power transfer,

$$R_L = R_{Th} = 9\ \Omega$$

and the maximum power is

$$p_{max} = \frac{V_{Th}^2}{4R_L} = \frac{22^2}{4 \times 9} = 13.44 \text{ W}$$

Practice Problem 4.13

Determine the value of R_L that will draw the maximum power from the rest of the circuit in Fig. 4.52. Calculate the maximum power.

Answer: 4.222 Ω, 2.901 W.

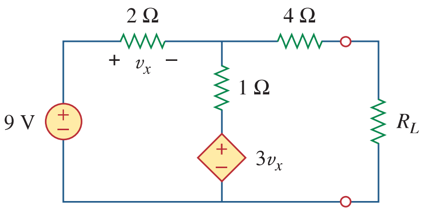

Figure 4.52
For Practice Prob. 4.13.

4.9 Verifying Circuit Theorems with *PSpice*

In this section, we learn how to use *PSpice* to verify the theorems covered in this chapter. Specifically, we will consider using DC Sweep analysis to find the Thevenin or Norton equivalent at any pair of nodes in a circuit and the maximum power transfer to a load. The reader is advised to read Section D.3 of Appendix D in preparation for this section.

To find the Thevenin equivalent of a circuit at a pair of open terminals using *PSpice*, we use the schematic editor to draw the circuit and insert an independent probing current source, say, Ip, at the terminals. The probing current source must have a part name ISRC. We then perform a DC Sweep on Ip, as discussed in Section D.3. Typically, we may let the current through Ip vary from 0 to 1 A in 0.1-A increments. After saving and simulating the circuit, we use Probe to display a plot of the voltage across Ip versus the current through Ip. The zero intercept of the plot gives us the Thevenin equivalent voltage, while the slope of the plot is equal to the Thevenin resistance.

To find the Norton equivalent involves similar steps except that we insert a probing independent voltage source (with a part name VSRC), say, Vp, at the terminals. We perform a DC Sweep on Vp and let Vp vary from 0 to 1 V in 0.1-V increments. A plot of the current through Vp versus the voltage across Vp is obtained using the Probe menu after simulation. The zero intercept is equal to the Norton current, while the slope of the plot is equal to the Norton conductance.

To find the maximum power transfer to a load using *PSpice* involves performing a DC parametric Sweep on the component value of R_L in Fig. 4.48 and plotting the power delivered to the load as a function of R_L. According to Fig. 4.49, the maximum power occurs when $R_L = R_{Th}$. This is best illustrated with an example, and Example 4.15 provides one.

We use VSRC and ISRC as part names for the independent voltage and current sources, respectively.

Example 4.14

Consider the circuit in Fig. 4.31 (see Example 4.9). Use *PSpice* to find the Thevenin and Norton equivalent circuits.

Solution:

(a) To find the Thevenin resistance R_{Th} and Thevenin voltage V_{Th} at the terminals *a-b* in the circuit in Fig. 4.31, we first use Schematics to draw the circuit as shown in Fig. 4.53(a). Notice that a probing current source I2 is inserted at the terminals. Under **Analysis/Setput**, we select DC Sweep. In the DC Sweep dialog box, we select Linear for the *Sweep Type* and Current Source for the *Sweep Var. Type*. We enter I2 under the *Name* box, 0 as *Start Value*, 1 as *End Value*, and 0.1 as *Increment*. After simulation, we add trace V(I2:–) from the *PSpice* A/D window and obtain the plot shown in Fig. 4.53(b). From the plot, we obtain

$$V_{Th} = \text{Zero intercept} = 20 \text{ V}, \qquad R_{Th} = \text{Slope} = \frac{26 - 20}{1} = 6\ \Omega$$

These agree with what we got analytically in Example 4.9.

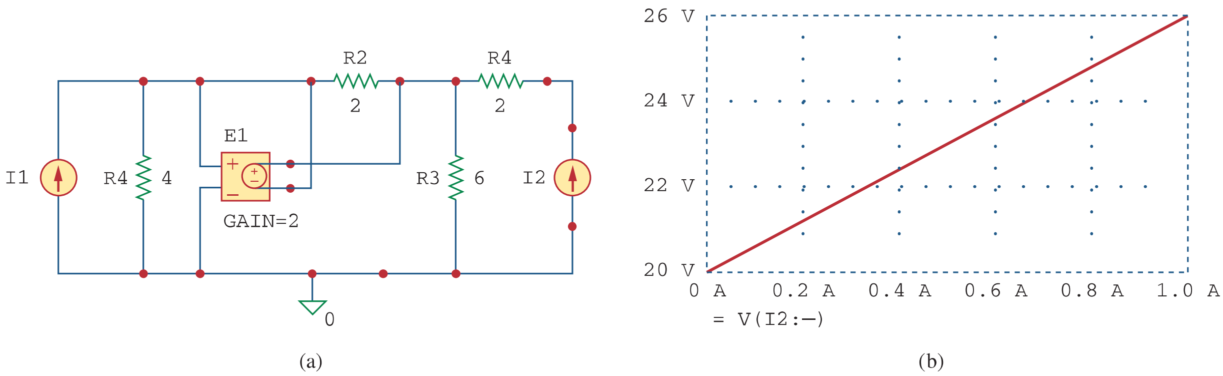

Figure 4.53
For Example 4.14: (a) schematic and (b) plot for finding R_{Th} and V_{Th}.

(b) To find the Norton equivalent, we modify the schematic in Fig. 4.53(a) by replaying the probing current source with a probing voltage source V1. The result is the schematic in Fig. 4.54(a). Again, in the DC Sweep dialog box, we select Linear for the *Sweep Type* and Voltage Source for the *Sweep Var. Type*. We enter V1 under *Name* box, 0 as *Start Value*, 1 as *End Value*, and 0.1 as *Increment*. Under the *PSpice* A/D Window, we add trace I (V1) and obtain the plot in Fig. 4.54(b). From the plot, we obtain

$$I_N = \text{Zero intercept} = 3.335 \text{ A}$$

$$G_N = \text{Slope} = \frac{3.335 - 3.165}{1} = 0.17 \text{ S}$$

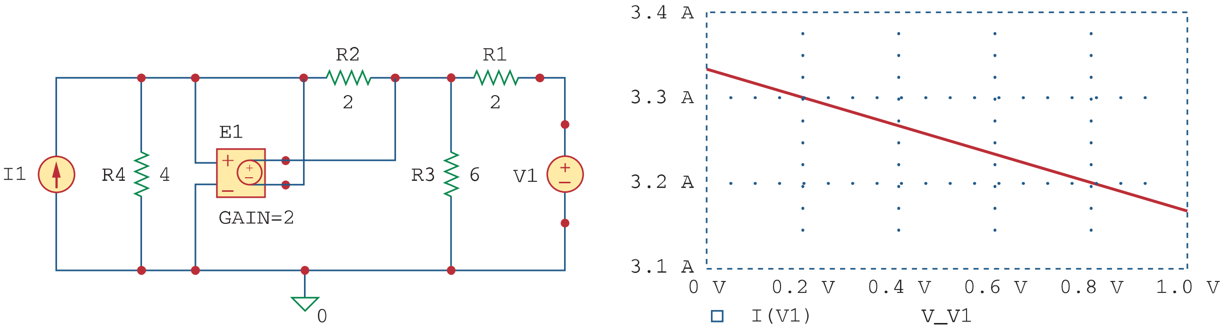

Figure 4.54
For Example 4.14: (a) schematic and (b) plot for finding G_N and I_N.

Practice Problem 4.14

Rework Practice Prob. 4.9 using *PSpice*.

Answer: $V_{\text{Th}} = 5.333$ V, $R_{\text{Th}} = 444.4$ mΩ.

Example 4.15

Refer to the circuit in Fig. 4.55. Use *PSpice* to find the maximum power transfer to R_L.

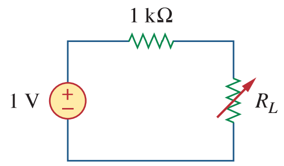

Figure 4.55
For Example 4.15.

Solution:

We need to perform a DC Sweep on R_L to determine when the power across it is maximum. We first draw the circuit using Schematics as shown in Fig. 4.56. Once the circuit is drawn, we take the following three steps to further prepare the circuit for a DC Sweep.

The first step involves defining the value of R_L as a parameter, since we want to vary it. To do this:

1. **DCLICKL** the value 1k of R2 (representing R_L) to open up the *Set Attribute Value* dialog box.
2. Replace 1k with {RL} and click **OK** to accept the change.

Note that the curly brackets are necessary.

The second step is to define parameter. To achieve this:

1. Select **Draw/Get New Part/Libraries** ···**/special.slb**.
2. Type PARAM in the *PartName* box and click **OK**.
3. **DRAG** the box to any position near the circuit.
4. **CLICKL** to end placement mode.
5. **DCLICKL** to open up the *PartName: PARAM* dialog box.
6. **CLICKL** on *NAME1* = and enter RL (with no curly brackets) in the *Value* box, and **CLICKL Save Attr** to accept change.
7. **CLICKL** on *VALUE1* = and enter 2k in the *Value* box, and **CLICKL Save Attr** to accept change.
8. Click **OK**.

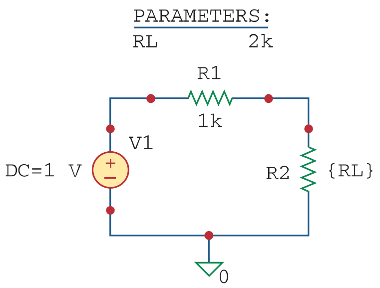

Figure 4.56
Schematic for the circuit in Fig. 4.55.

The value 2k in item 7 is necessary for a bias point calculation; it cannot be left blank.

The third step is to set up the DC Sweep to sweep the parameter. To do this:

1. Select **Analysis/Setput** to bring up the DC Sweep dialog box.
2. For the *Sweep Type*, select Linear (or Octave for a wide range of R_L).
3. For the *Sweep Var. Type*, select Global Parameter.
4. Under the *Name* box, enter RL.
5. In the *Start Value* box, enter 100.
6. In the *End Value* box, enter 5k.
7. In the *Increment* box, enter 100.
8. Click **OK** and **Close** to accept the parameters.

After taking these steps and saving the circuit, we are ready to simulate. Select **Analysis/Simulate**. If there are no errors, we select **Add Trace** in the *PSpice* A/D window and type −V(R2:2)*I(R2) in the *Trace Command* box. [The negative sign is needed since I(R2) is negative.] This gives the plot of the power delivered to R_L as R_L varies from 100 Ω to 5 kΩ. We can also obtain the power absorbed by R_L by typing V(R2:2)*V(R2:2)/RL in the *Trace Command* box. Either way, we obtain the plot in Fig. 4.57. It is evident from the plot that the maximum power is 250 μW. Notice that the maximum occurs when $R_L = 1$ kΩ, as expected analytically.

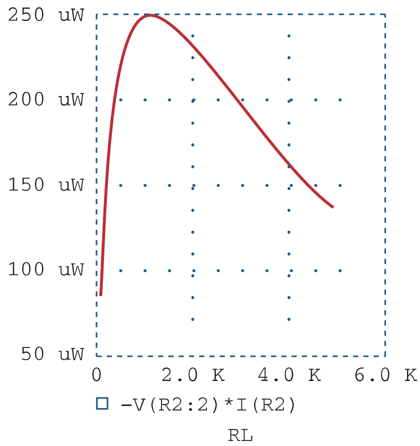

Figure 4.57
For Example 4.15: the plot of power across R_L.

Practice Problem 4.15

Find the maximum power transferred to R_L if the 1-kΩ resistor in Fig. 4.55 is replaced by a 2-kΩ resistor.

Answer: 125 μW.

4.10 †Applications

In this section we will discuss two important practical applications of the concepts covered in this chapter: source modeling and resistance measurement.

4.10.1 Source Modeling

Source modeling provides an example of the usefulness of the Thevenin or the Norton equivalent. An active source such as a battery is often characterized by its Thevenin or Norton equivalent circuit. An ideal voltage source provides a constant voltage irrespective of the current drawn by the load, while an ideal current source supplies a constant current regardless of the load voltage. As Fig. 4.58 shows, practical voltage and current sources are not ideal, due to their *internal resistances* or *source resistances* R_s and R_p. They become ideal as $R_s \rightarrow 0$ and $R_p \rightarrow \infty$. To show that this is the case, consider the effect

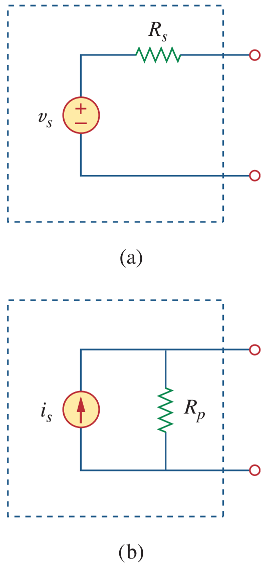

Figure 4.58
(a) Practical voltage source, (b) practical current source.

of the load on voltage sources, as shown in Fig. 4.59(a). By the voltage division principle, the load voltage is

$$v_L = \frac{R_L}{R_s + R_L} v_s \tag{4.25}$$

As R_L increases, the load voltage approaches a source voltage v_s, as illustrated in Fig. 4.59(b). From Eq. (4.25), we should note that:

1. The load voltage will be constant if the internal resistance R_s of the source is zero or, at least, $R_s \ll R_L$. In other words, the smaller R_s is compared with R_L, the closer the voltage source is to being ideal.

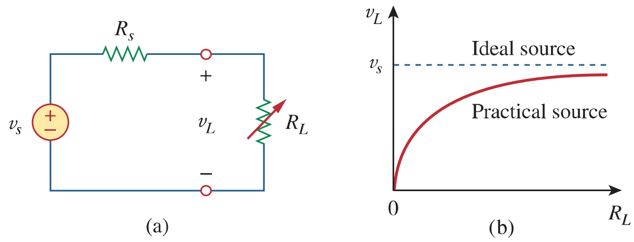

Figure 4.59
(a) Practical voltage source connected to a load R_L, (b) load voltage decreases as R_L decreases.

2. When the load is disconnected (i.e., the source is open-circuited so that $R_L \to \infty$), $v_{oc} = v_s$. Thus, v_s may be regarded as the *unloaded source* voltage. The connection of the load causes the terminal voltage to drop in magnitude; this is known as the *loading effect*.

The same argument can be made for a practical current source when connected to a load as shown in Fig. 4.60(a). By the current division principle,

$$i_L = \frac{R_p}{R_p + R_L} i_s \tag{4.26}$$

Figure 4.60(b) shows the variation in the load current as the load resistance increases. Again, we notice a drop in current due to the load (loading effect), and load current is constant (ideal current source) when the internal resistance is very large (i.e., $R_p \to \infty$ or, at least, $R_p \gg R_L$).

Sometimes, we need to know the unloaded source voltage v_s and the internal resistance R_s of a voltage source. To find v_s and R_s, we follow the procedure illustrated in Fig. 4.61. First, we measure the open-circuit voltage v_{oc} as in Fig. 4.61(a) and set

$$v_s = v_{oc} \tag{4.27}$$

Then, we connect a variable load R_L across the terminals as in Fig. 4.61(b). We adjust the resistance R_L until we measure a load voltage of exactly one-half of the open-circuit voltage, $v_L = v_{oc}/2$, because now $R_L = R_{Th} = R_s$. At that point, we disconnect R_L and measure it. We set

$$R_s = R_L \tag{4.28}$$

For example, a car battery may have $v_s = 12$ V and $R_s = 0.05\ \Omega$.

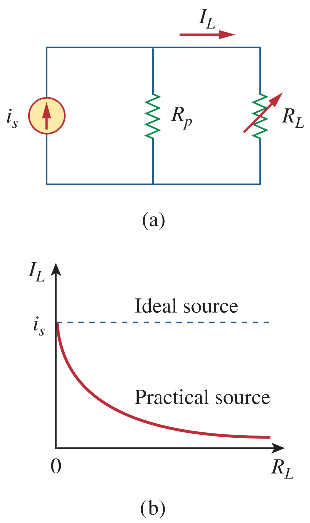

Figure 4.60
(a) Practical current source connected to a load R_L, (b) load current decreases as R_L increases.

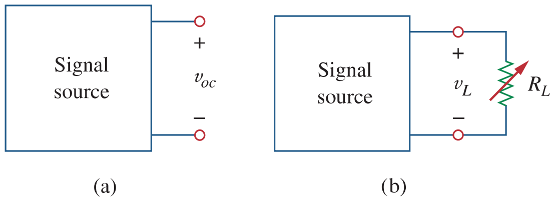

Figure 4.61
(a) Measuring v_{oc}, (b) measuring v_L.

Example 4.16

The terminal voltage of a voltage source is 12 V when connected to a 2-W load. When the load is disconnected, the terminal voltage rises to 12.4 V. (a) Calculate the source voltage v_s and internal resistance R_s. (b) Determine the voltage when an 8-Ω load is connected to the source.

Solution:

(a) We replace the source by its Thevenin equivalent. The terminal voltage when the load is disconnected is the open-circuit voltage,

$$v_s = v_{oc} = 12.4 \text{ V}$$

When the load is connected, as shown in Fig. 4.62(a), $v_L = 12$ V and $p_L = 2$ W. Hence,

$$p_L = \frac{v_L^2}{R_L} \quad \Rightarrow \quad R_L = \frac{v_L^2}{p_L} = \frac{12^2}{2} = 72 \ \Omega$$

The load current is

$$i_L = \frac{v_L}{R_L} = \frac{12}{72} = \frac{1}{6} \text{ A}$$

The voltage across R_s is the difference between the source voltage v_s and the load voltage v_L, or

$$12.4 - 12 = 0.4 = R_s i_L, \qquad R_s = \frac{0.4}{I_L} = 2.4 \ \Omega$$

(b) Now that we have the Thevenin equivalent of the source, we connect the 8-Ω load across the Thevenin equivalent as shown in Fig. 4.62(b). Using voltage division, we obtain

$$v = \frac{8}{8 + 2.4}(12.4) = 9.538 \text{ V}$$

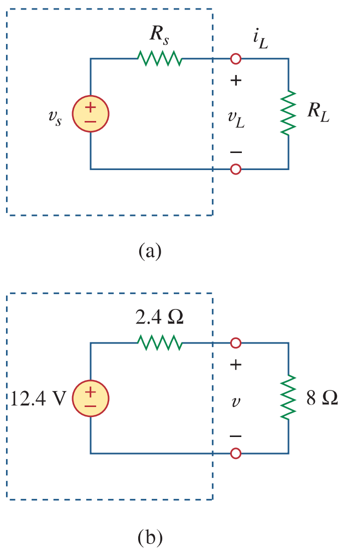

Figure 4.62
For Example 4.16.

Practice Problem 4.16

The measured open-circuit voltage across a certain amplifier is 9 V. The voltage drops to 8 V when a 20-Ω loudspeaker is connected to the amplifier. Calculate the voltage when a 10-Ω loudspeaker is used instead.

Answer: 7.2 V.

4.10.2 Resistance Measurement

Although the ohmmeter method provides the simplest way to measure resistance, more accurate measurement may be obtained using the Wheatstone bridge. While ohmmeters are designed to measure resistance in low, mid, or high range, a Wheatstone bridge is used to measure resistance in the mid range, say, between 1 Ω and 1 MΩ. Very low values of resistances are measured with a *milliohmmeter*, while very high values are measured with a *Megger tester.*

Historical note: The bridge was invented by Charles Wheatstone (1802–1875), a British professor who also invented the telegraph, as Samuel Morse did independently in the United States.

The Wheatstone bridge (or resistance bridge) circuit is used in a number of applications. Here we will use it to measure an unknown resistance. The unknown resistance R_x is connected to the bridge as shown in Fig. 4.63. The variable resistance is adjusted until no current flows through the galvanometer, which is essentially a d'Arsonval movement operating as a sensitive current-indicating device like an ammeter in the microamp range. Under this condition $v_1 = v_2$, and the bridge is said to be *balanced*. Since no current flows through the galvanometer, R_1 and R_2 behave as though they were in series; so do R_3 and R_x. The fact that no current flows through the galvanometer also implies that $v_1 = v_2$. Applying the voltage division principle,

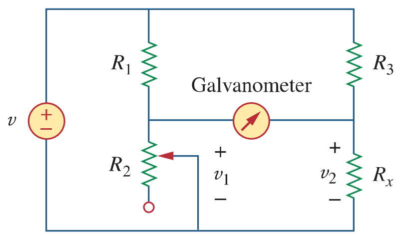

Figure 4.63
The Wheatstone bridge; R_x is the resistance to be measured.

$$v_1 = \frac{R_2}{R_1 + R_2}v = v_2 = \frac{R_x}{R_3 + R_x}v \tag{4.29}$$

Hence, no current flows through the galvanometer when

$$\frac{R_2}{R_1 + R_2} = \frac{R_x}{R_3 + R_x} \quad \Rightarrow \quad R_2R_3 = R_1R_x$$

or

$$\boxed{R_x = \frac{R_3}{R_1}R_2} \tag{4.30}$$

If $R_1 = R_3$, and R_2 is adjusted until no current flows through the galvanometer, then $R_x = R_2$.

How do we find the current through the galvanometer when the Wheatstone bridge is *unbalanced*? We find the Thevenin equivalent (V_{Th} and R_{Th}) with respect to the galvanometer terminals. If R_m is the resistance of the galvanometer, the current through it under the unbalanced condition is

$$I = \frac{V_{\text{Th}}}{R_{\text{Th}} + R_m} \tag{4.31}$$

Example 4.18 will illustrate this.

Example 4.17

In Fig. 4.63, $R_1 = 500\ \Omega$ and $R_3 = 200\ \Omega$. The bridge is balanced when R_2 is adjusted to be 125 Ω. Determine the unknown resistance R_x.

Solution:
Using Eq. (4.30) gives

$$R_x = \frac{R_3}{R_1}R_2 = \frac{200}{500}125 = 50\ \Omega$$

Practice Problem 4.17

A Wheatstone bridge has $R_1 = R_3 = 1\ \text{k}\Omega$. R_2 is adjusted until no current flows through the galvanometer. At that point, $R_2 = 3.2\ \text{k}\Omega$. What is the value of the unknown resistance?

Answer: 3.2 kΩ.

Example 4.18

The circuit in Fig. 4.64 represents an unbalanced bridge. If the galvanometer has a resistance of 40 Ω, find the current through the galvanometer.

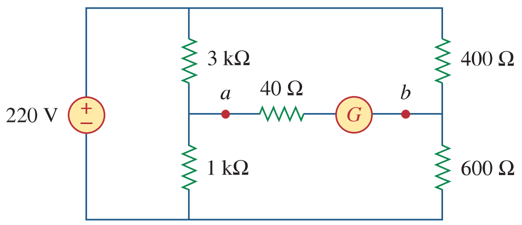

Figure 4.64
Unbalanced bridge of Example 4.18.

Solution:
We first need to replace the circuit by its Thevenin equivalent at terminals a and b. The Thevenin resistance is found using the circuit in Fig. 4.65(a). Notice that the 3-kΩ and 1-kΩ resistors are in parallel; so are the 400-Ω and 600-Ω resistors. The two parallel combinations form a series combination with respect to terminals a and b. Hence,

$$R_{\text{Th}} = 3000 \parallel 1000 + 400 \parallel 600$$
$$= \frac{3000 \times 1000}{3000 + 1000} + \frac{400 \times 600}{400 + 600} = 750 + 240 = 990\ \Omega$$

To find the Thevenin voltage, we consider the circuit in Fig. 4.65(b). Using the voltage division principle gives

$$v_1 = \frac{1000}{1000 + 3000}(220) = 55\ \text{V}, \qquad v_2 = \frac{600}{600 + 400}(220) = 132\ \text{V}$$

Applying KVL around loop ab gives

$$-v_1 + V_{\text{Th}} + v_2 = 0 \qquad \text{or} \qquad V_{\text{Th}} = v_1 - v_2 = 55 - 132 = -77\ \text{V}$$

Having determined the Thevenin equivalent, we find the current through the galvanometer using Fig. 4.65(c).

$$I_G = \frac{V_{\text{Th}}}{R_{\text{Th}} + R_m} = \frac{-77}{990 + 40} = -74.76\ \text{mA}$$

The negative sign indicates that the current flows in the direction opposite to the one assumed, that is, from terminal b to terminal a.

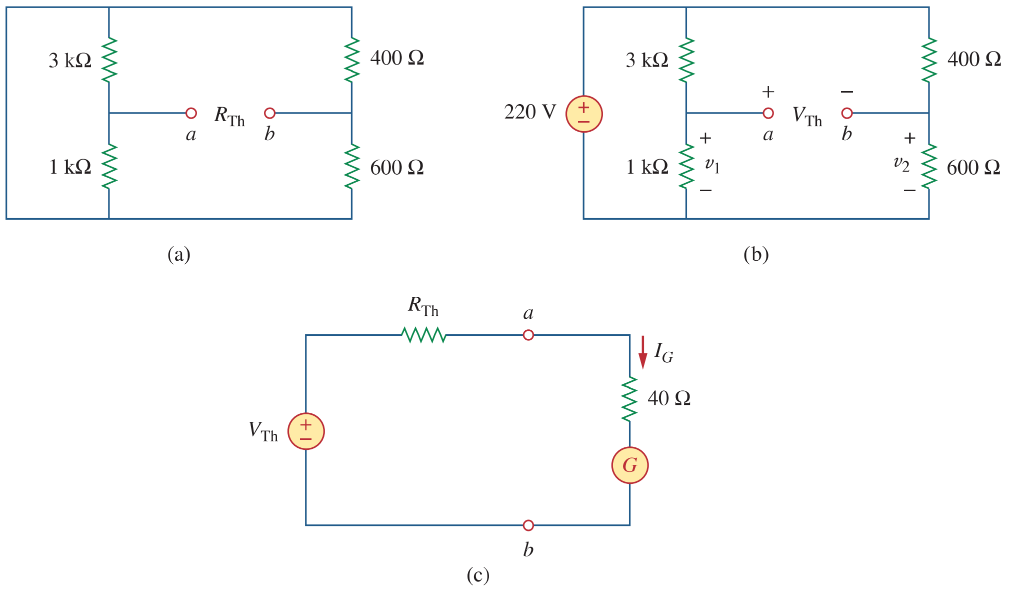

Figure 4.65
For Example 4.18: (a) Finding R_{Th}, (b) finding V_{Th}, (c) determining the current through the galvanometer.

Practice Problem 4.18

Obtain the current through the galvanometer, having a resistance of 14 Ω, in the Wheatstone bridge shown in Fig. 4.66.

Answer: 64 mA.

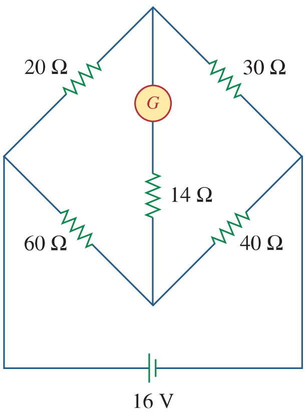

Figure 4.66
For Practice Prob. 4.18.

4.11 Summary

1. A linear network consists of linear elements, linear dependent sources, and linear independent sources.
2. Network theorems are used to reduce a complex circuit to a simpler one, thereby making circuit analysis much simpler.
3. The superposition principle states that for a circuit having multiple independent sources, the voltage across (or current through) an element is equal to the algebraic sum of all the individual voltages (or currents) due to each independent source acting one at a time.
4. Source transformation is a procedure for transforming a voltage source in series with a resistor to a current source in parallel with a resistor, or vice versa.
5. Thevenin's and Norton's theorems allow us to isolate a portion of a network while the remaining portion of the network is replaced by an equivalent network. The Thevenin equivalent consists of a voltage source V_{Th} in series with a resistor R_{Th}, while the Norton equivalent consists of a current source I_N in parallel with a resistor R_N. The two theorems are related by source transformation.

$$R_N = R_{Th}, \qquad I_N = \frac{V_{Th}}{R_{Th}}$$

6. For a given Thevenin equivalent circuit, maximum power transfer occurs when $R_L = R_{Th}$; that is, when the load resistance is equal to the Thevenin resistance.
7. The maximum power transfer theorem states that the maximum power is delivered by a source to the load R_L when R_L is equal to R_{Th}, the Thevenin resistance at the terminals of the load.
8. *PSpice* can be used to verify the circuit theorems covered in this chapter.
9. Source modeling and resistance measurement using the Wheatstone bridge provide applications for Thevenin's theorem.

Review Questions

4.1 The current through a branch in a linear network is 2 A when the input source voltage is 10 V. If the voltage is reduced to 1 V and the polarity is reversed, the current through the branch is:

(a) −2 A (b) −0.2 A (c) 0.2 A
(d) 2 A (e) 20 A

4.2 For superposition, it is not required that only one independent source be considered at a time; any number of independent sources may be considered simultaneously.

(a) True (b) False

4.3 The superposition principle applies to power calculation.

(a) True (b) False

4.4 Refer to Fig. 4.67. The Thevenin resistance at terminals *a* and *b* is:

(a) 25 Ω (b) 20 Ω
(c) 5 Ω (d) 4 Ω

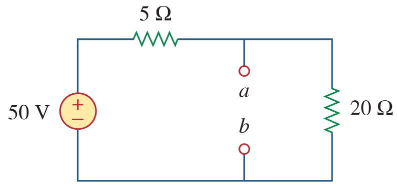

Figure 4.67
For Review Questions 4.4 to 4.6.

4.5 The Thevenin voltage across terminals *a* and *b* of the circuit in Fig. 4.67 is:

(a) 50 V (b) 40 V
(c) 20 V (d) 10 V

4.6 The Norton current at terminals *a* and *b* of the circuit in Fig. 4.67 is:

(a) 10 A (b) 2.5 A
(c) 2 A (d) 0 A

4.7 The Norton resistance R_N is exactly equal to the Thevenin resistance R_{Th}.

(a) True (b) False

4.8 Which pair of circuits in Fig. 4.68 are equivalent?

(a) a and b (b) b and d
(c) a and c (d) c and d

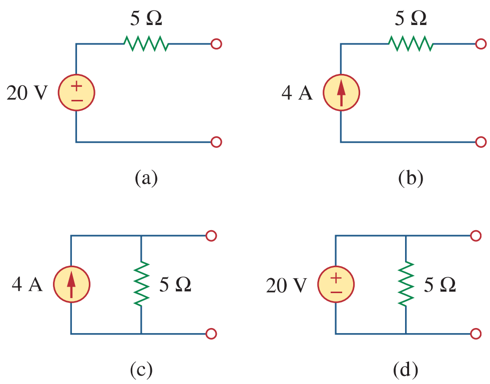

Figure 4.68
For Review Question 4.8.

4.9 A load is connected to a network. At the terminals to which the load is connected, $R_{Th} = 10\ \Omega$ and $V_{Th} = 40$ V. The maximum possible power supplied to the load is:

(a) 160 W (b) 80 W
(c) 40 W (d) 1 W

4.10 The source is supplying the maximum power to the load when the load resistance equals the source resistance.

(a) True (b) False

Answers: 4.1b, 4.2a, 4.3b, 4.4d, 4.5b, 4.6a, 4.7a, 4.8c, 4.9c, 4.10a.

Problems

Section 4.2 Linearity Property

4.1 Calculate the current i_o in the circuit of Fig. 4.69. What value of input voltage is necessary to make i_o equal to 5 amps?

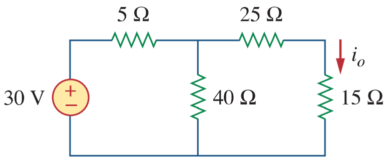

Figure 4.69
For Prob. 4.1.

4.2 Using Fig. 4.70, design a problem to help other students better understand linearity.

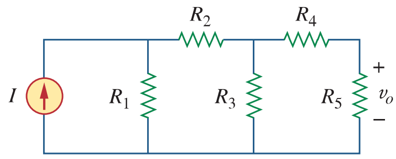

Figure 4.70
For Prob. 4.2.

4.3 (a) In the circuit of Fig. 4.71, calculate v_o and i_o when $v_s = 1$ V.

(b) Find v_o and i_o when $v_s = 10$ V.

(c) What are v_o and i_o when each of the 1-Ω resistors is replaced by a 10-Ω resistor and $v_s = 10$ V?

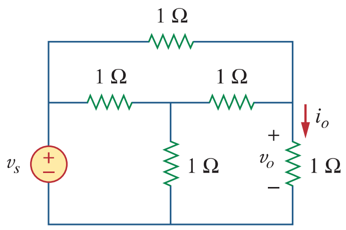

Figure 4.71
For Prob. 4.3.

4.4 Use linearity to determine i_o in the circuit of Fig. 4.72.

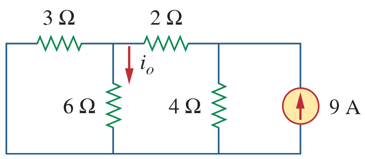

Figure 4.72
For Prob. 4.4.

4.5 For the circuit in Fig. 4.73, assume $v_o = 1$ V, and use linearity to find the actual value of v_o.

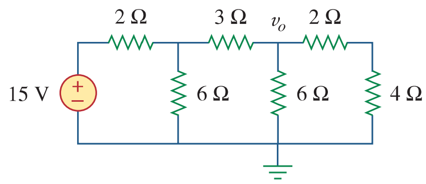

Figure 4.73
For Prob. 4.5.

4.6 For the linear circuit shown in Fig. 4.74, use linearity to complete the following table.

Experiment	V_s	V_o
1	12 V	4 V
2		16 V
3	1 V	
4		−2 V

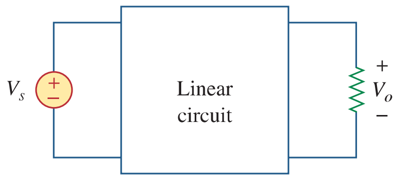

Figure 4.74
For Prob. 4.6.

4.7 Use linearity and the assumption that $V_o = 1$ V to find the actual value of V_o in Fig. 4.75.

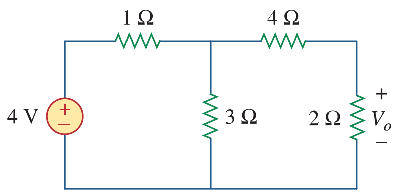

Figure 4.75
For Prob. 4.7.

Section 4.3 Superposition

4.8 Using superposition, find V_o in the circuit of Fig. 4.76. Check with *PSpice or MultiSim.*

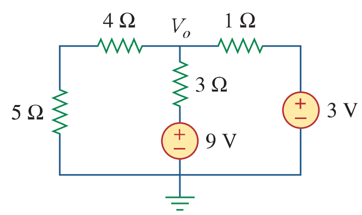

Figure 4.76
For Prob. 4.8.

4.9 Given that $I = 4$ amps when $V_s = 40$ volts and $I_s = 4$ amps and $I = 1$ amp when $V_s = 20$ volts and $I_s = 0$, use superposition and linearity to determine the value of I when $V_s = 60$ volts and $I_s = -2$ amps.

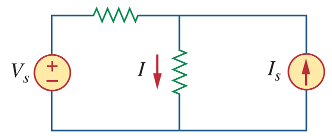

Figure 4.77
For Prob. 4.9.

4.10 Using Fig. 4.78, design a problem to help other students better understand superposition. Note, the letter k is a gain you can specify to make the problem easier to solve but must not be zero.

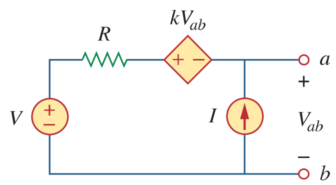

Figure 4.78
For Prob. 4.10.

4.11 Use the superposition principle to find i_o and v_o in the circuit of Fig. 4.79.

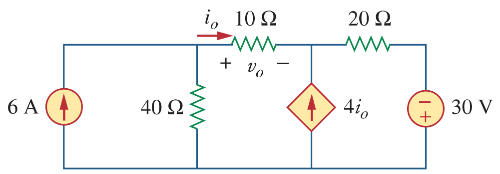

Figure 4.79
For Prob. 4.11.

4.12 Determine v_o in the circuit of Fig. 4.80 using the superposition principle.

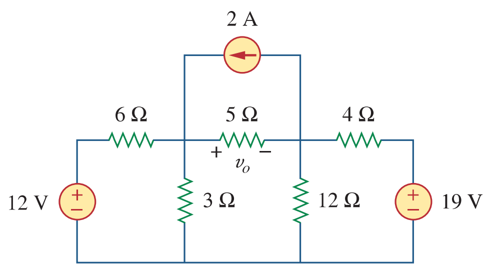

Figure 4.80
For Prob. 4.12.

4.13 Use superposition to find v_o in the circuit of Fig. 4.81.

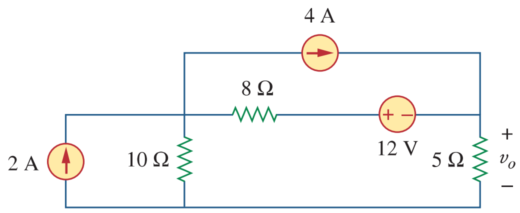

Figure 4.81
For Prob. 4.13.

4.14 Apply the superposition principle to find v_o in the circuit of Fig. 4.82.

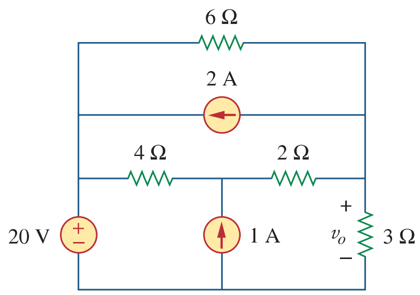

Figure 4.82
For Prob. 4.14.

4.15 For the circuit in Fig. 4.83, use superposition to find i. Calculate the power delivered to the 3-Ω resistor.

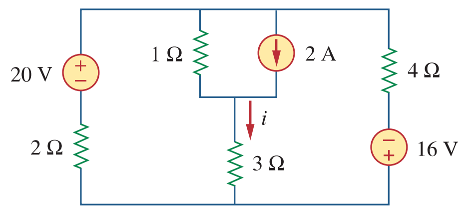

Figure 4.83
For Probs. 4.15 and 4.56.

4.16 Given the circuit in Fig. 4.84, use superposition to obtain i_0.

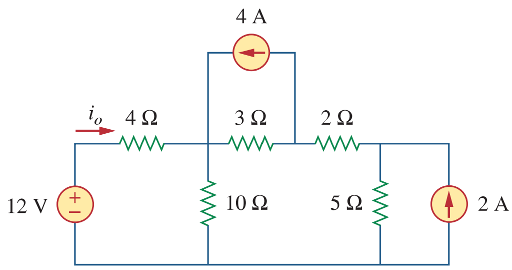

Figure 4.84
For Prob. 4.16.

4.17 Use superposition to obtain v_x in the circuit of Fig. 4.85. Check your result using *PSpice or MultiSim.*

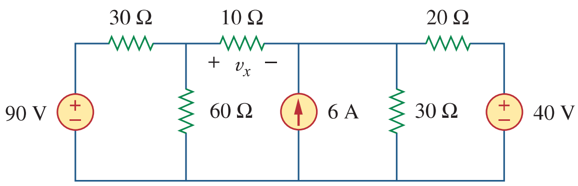

Figure 4.85
For Prob. 4.17.

4.18 Use superposition to find V_o in the circuit of Fig. 4.86.

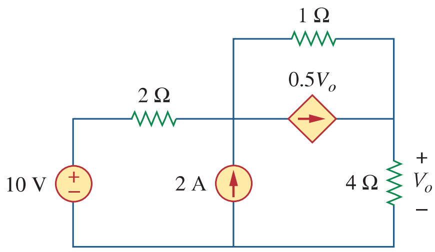

Figure 4.86
For Prob. 4.18.

4.19 Use superposition to solve for v_x in the circuit of Fig. 4.87.

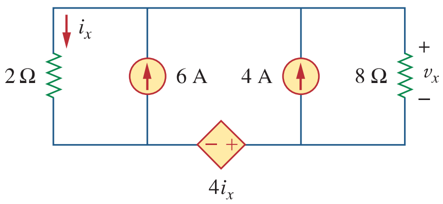

Figure 4.87
For Prob. 4.19.

Section 4.4 Source Transformation

4.20 Use source transformation to reduce the circuit in Fig. 4.88 to a single voltage source in series with a single resistor.

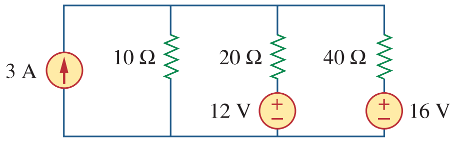

Figure 4.88
For Prob. 4.20.

4.21 Using Fig. 4.89, design a problem to help other students better understand source transformation.

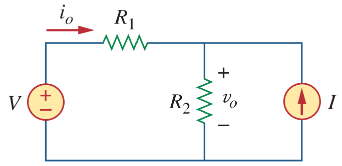

Figure 4.89
For Prob. 4.21.

4.22 For the circuit in Fig. 4.90, use source transformation to find i.

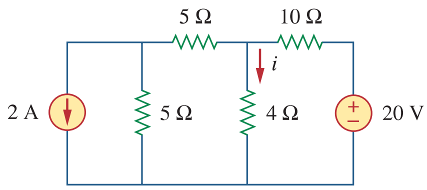

Figure 4.90
For Prob. 4.22.

4.23 Referring to Fig. 4.91, use source transformation to determine the current and power absorbed by the 8-Ω resistor.

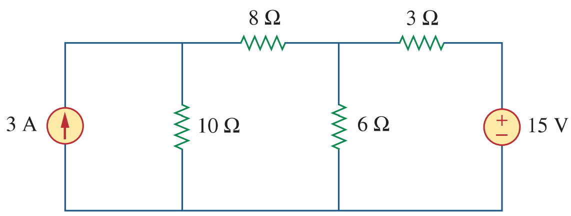

Figure 4.91
For Prob. 4.23.

4.24 Use source transformation to find the voltage V_x in the circuit of Fig. 4.92.

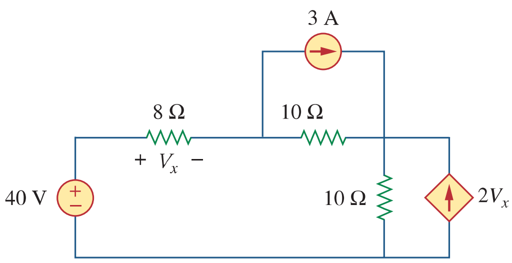

Figure 4.92
For Prob. 4.24.

4.25 Obtain v_o in the circuit of Fig. 4.93 using source transformation. Check your result using *PSpice or MultiSim.*

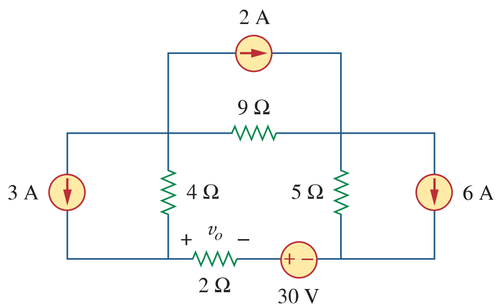

Figure 4.93
For Prob. 4.25.

4.26 Use source transformation to find i_o in the circuit of Fig. 4.94.

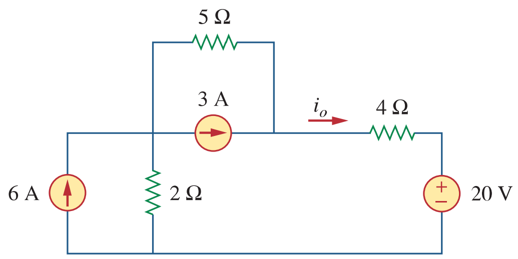

Figure 4.94
For Prob. 4.26.

4.27 Apply source transformation to find v_x in the circuit of Fig. 4.95.

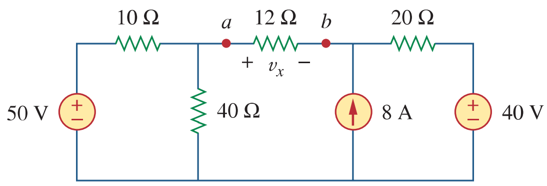

Figure 4.95
For Probs. 4.27 and 4.40.

4.28 Use source transformation to find I_o in Fig. 4.96.

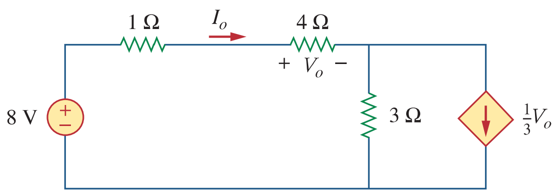

Figure 4.96
For Prob. 4.28.

4.29 Use source transformation to find v_o in the circuit of Fig. 4.97.

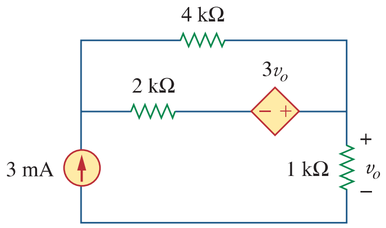

Figure 4.97
For Prob. 4.29.

4.30 Use source transformation on the circuit shown in Fig 4.98 to find i_x.

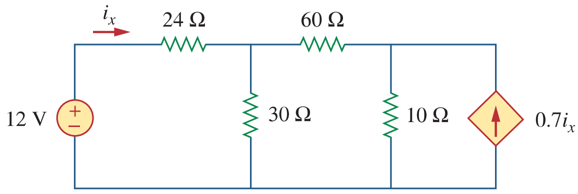

Figure 4.98
For Prob. 4.30.

4.31 Determine v_x in the circuit of Fig. 4.99 using source transformation.

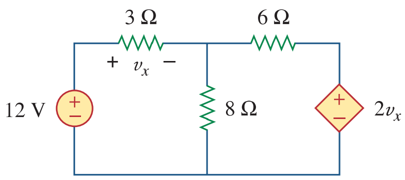

Figure 4.99
For Prob. 4.31.

4.32 Use source transformation to find i_x in the circuit of Fig. 4.100.

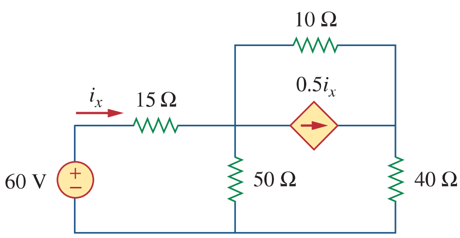

Figure 4.100
For Prob. 4.32.

Sections 4.5 and 4.6 Thevenin's and Norton's Theorems

4.33 Determine the Thevenin equivalent circuit, shown in Fig. 4.101, as seen by the 5-ohm resistor.

Then calculate the current flowing through the 5-ohm resistor.

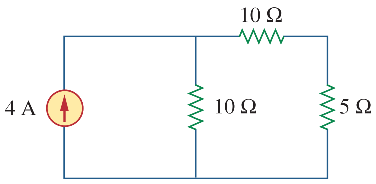

Figure 4.101
For Prob. 4.33.

4.34 Using Fig. 4.102, design a problem that will help other students better understand Thevenin equivalent circuits.

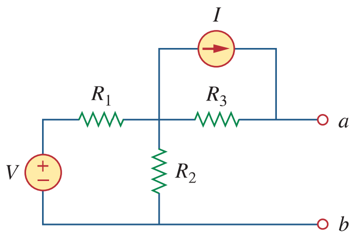

Figure 4.102
For Probs. 4.34 and 4.49.

4.35 Use Thevenin's theorem to find v_o in Prob. 4.12.

4.36 Solve for the current i in the circuit of Fig. 4.103 using Thevenin's theorem. (*Hint:* Find the Thevenin equivalent seen by the 12-Ω resistor.)

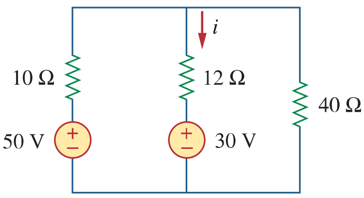

Figure 4.103
For Prob. 4.36.

4.37 Find the Norton equivalent with respect to terminals *a-b* in the circuit shown in Fig. 4.104.

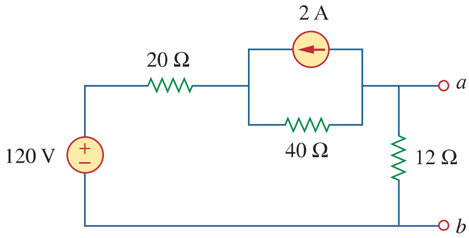

Figure 4.104
For Prob. 4.37.

4.38 Apply Thevenin's theorem to find V_o in the circuit of Fig. 4.105.

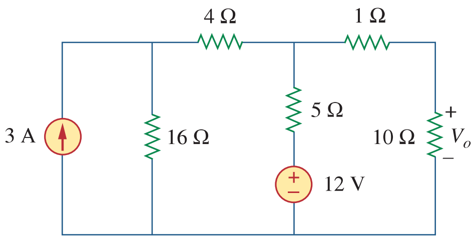

Figure 4.105
For Prob. 4.38.

4.39 Obtain the Thevenin equivalent at terminals *a-b* of the circuit shown in Fig. 4.106.

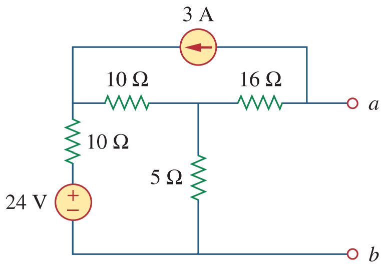

Figure 4.106
For Prob. 4.39.

4.40 Find the Thevenin equivalent at terminals *a-b* of the circuit in Fig. 4.107.

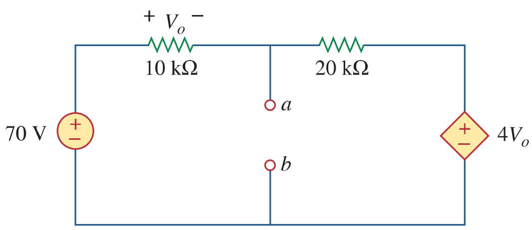

Figure 4.107
For Prob. 4.40.

4.41 Find the Thevenin and Norton equivalents at terminals *a-b* of the circuit shown in Fig. 4.108.

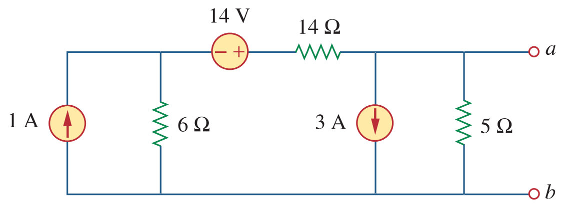

Figure 4.108
For Prob. 4.41.

***4.42** For the circuit in Fig. 4.109, find the Thevenin equivalent between terminals *a* and *b*.

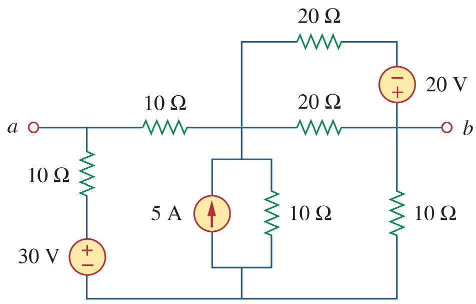

Figure 4.109
For Prob. 4.42.

4.43 Find the Thevenin equivalent looking into terminals *a-b* of the circuit in Fig. 4.110 and solve for i_x.

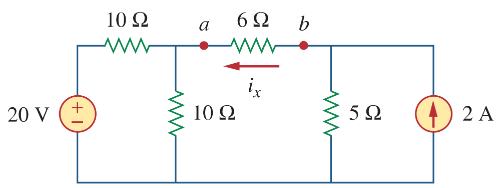

Figure 4.110
For Prob. 4.43.

4.44 For the circuit in Fig. 4.111, obtain the Thevenin equivalent as seen from terminals:

(a) *a-b* (b) *b-c*

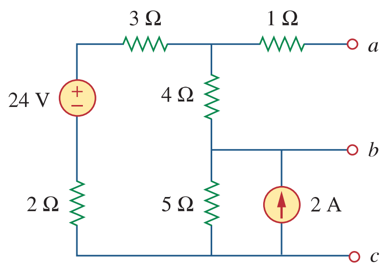

Figure 4.111
For Prob. 4.44.

* An asterisk indicates a challenging problem.

4.45 Find the Thevenin equivalent of the circuit in Fig. 4.112 as seen by looking into terminals *a* and *b*.

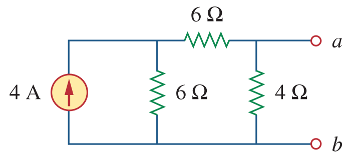

Figure 4.112
For Prob. 4.45.

4.46 Using Fig. 4.113, design a problem to help other students better understand Norton equivalent circuits.

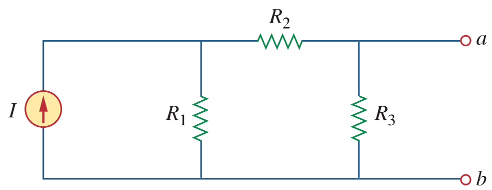

Figure 4.113
For Prob. 4.46.

4.47 Obtain the Thevenin and Norton equivalent circuits of the circuit in Fig. 4.114 with respect to terminals *a* and *b*.

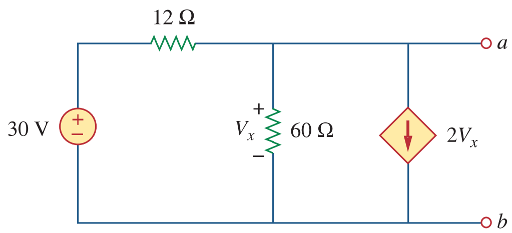

Figure 4.114
For Prob. 4.47.

4.48 Determine the Norton equivalent at terminals *a-b* for the circuit in Fig. 4.115.

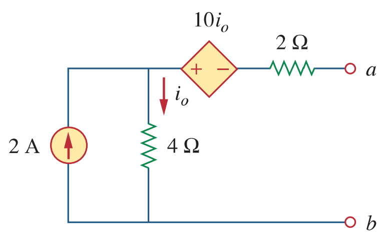

Figure 4.115
For Prob. 4.48.

4.49 Find the Norton equivalent looking into terminals *a-b* of the circuit in Fig. 4.102. Let $V = 40$ V, $I = 3$ A, $R_1 = 10\ \Omega$, $R_2 = 40\ \Omega$, and $R_3 = 20\ \Omega$.

4.50 Obtain the Norton equivalent of the circuit in Fig. 4.116 to the left of terminals a-b. Use the result to find current i.

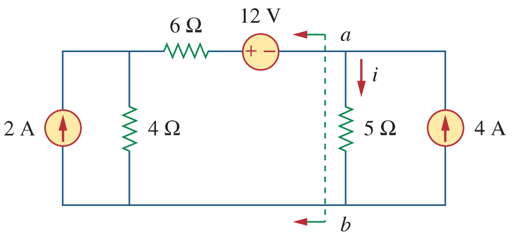

Figure 4.116
For Prob. 4.50.

4.51 Given the circuit in Fig. 4.117, obtain the Norton equivalent as viewed from terminals:

(a) a-b (b) c-d

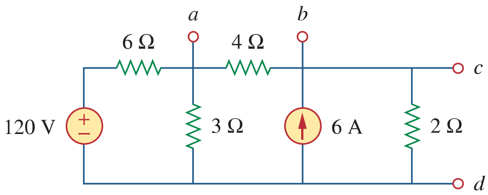

Figure 4.117
For Prob. 4.51.

4.52 For the transistor model in Fig. 4.118, obtain the Thevenin equivalent at terminals a-b.

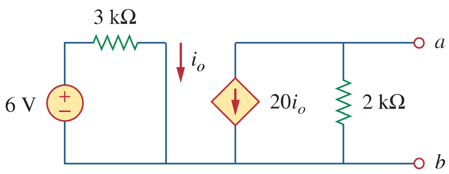

Figure 4.118
For Prob. 4.52.

4.53 Find the Norton equivalent at terminals a-b of the circuit in Fig. 4.119.

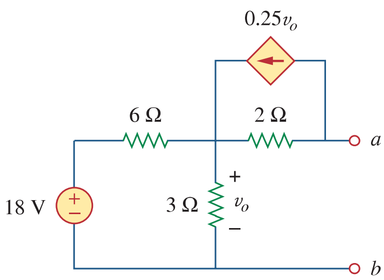

Figure 4.119
For Prob. 4.53.

4.54 Find the Thevenin equivalent between terminals a-b of the circuit in Fig. 4.120.

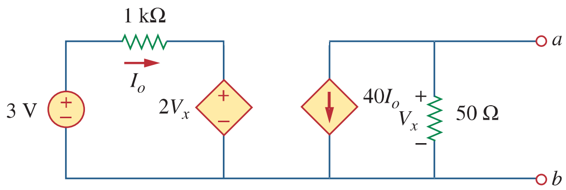

Figure 4.120
For Prob. 4.54.

***4.55** Obtain the Norton equivalent at terminals a-b of the circuit in Fig. 4.121.

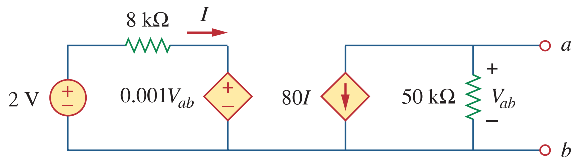

Figure 4.121
For Prob. 4.55.

4.56 Use Norton's theorem to find V_o in the circuit of Fig. 4.122.

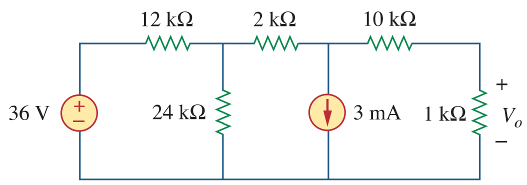

Figure 4.122
For Prob. 4.56.

4.57 Obtain the Thevenin and Norton equivalent circuits at terminals a-b for the circuit in Fig. 4.123.

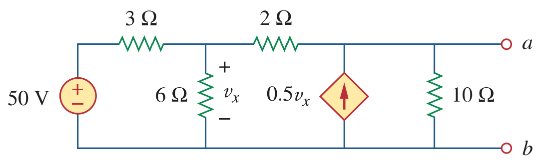

Figure 4.123
For Probs. 4.57 and 4.79.

4.58 The network in Fig. 4.124 models a bipolar transistor common-emitter amplifier connected to a load. Find the Thevenin resistance seen by the load.

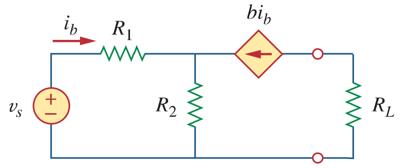

Figure 4.124
For Prob. 4.58.

4.59 Determine the Thevenin and Norton equivalents at terminals *a*-*b* of the circuit in Fig. 4.125.

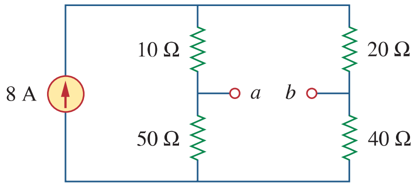

Figure 4.125
For Probs. 4.59 and 4.80.

***4.60** For the circuit in Fig. 4.126, find the Thevenin and Norton equivalent circuits at terminals *a*-*b*.

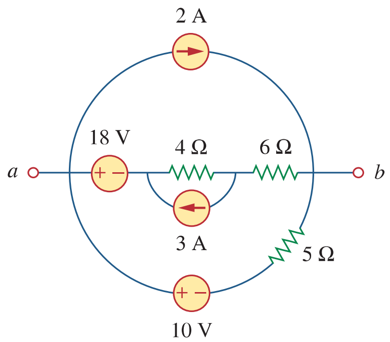

Figure 4.126
For Probs. 4.60 and 4.81.

***4.61** Obtain the Thevenin and Norton equivalent circuits at terminals *a*-*b* of the circuit in Fig. 4.127.

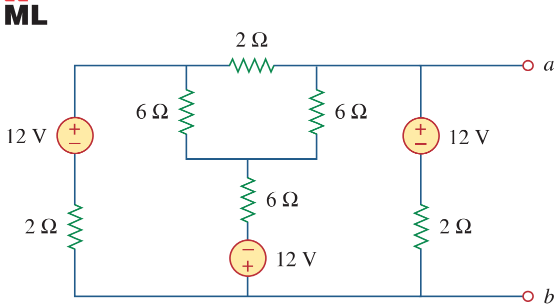

Figure 4.127
For Prob. 4.61.

***4.62** Find the Thevenin equivalent of the circuit in Fig. 4.128.

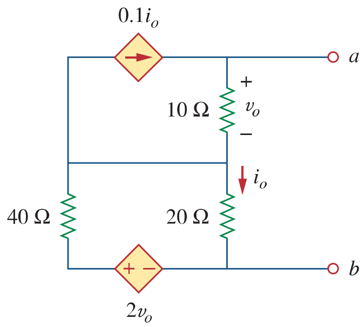

Figure 4.128
For Prob. 4.62.

4.63 Find the Norton equivalent for the circuit in Fig. 4.129.

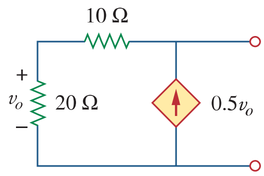

Figure 4.129
For Prob. 4.63.

4.64 Obtain the Thevenin equivalent seen at terminals *a*-*b* of the circuit in Fig. 4.130.

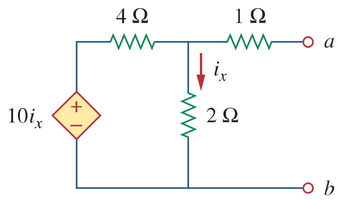

Figure 4.130
For Prob. 4.64.

4.65 For the circuit shown in Fig. 4.131, determine the relationship between V_o and I_o.

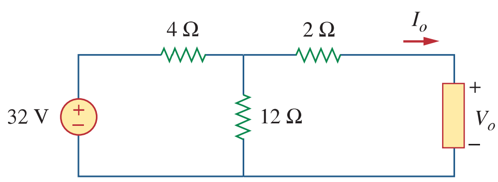

Figure 4.131
For Prob. 4.65.

Section 4.8 Maximum Power Transfer

4.66 Find the maximum power that can be delivered to the resistor R in the circuit of Fig. 4.132.

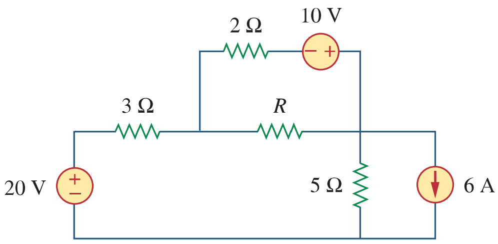

Figure 4.132
For Prob. 4.66.

4.67 The variable resistor R in Fig. 4.133 is adjusted until it absorbs the maximum power from the circuit.
(a) Calculate the value of R for maximum power.
(b) Determine the maximum power absorbed by R.

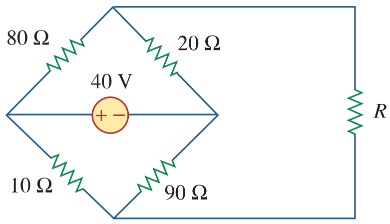

Figure 4.133
For Prob. 4.67.

***4.68** Compute the value of R that results in maximum power transfer to the 10-Ω resistor in Fig. 4.134. Find the maximum power.

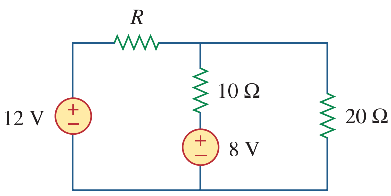

Figure 4.134
For Prob. 4.68.

4.69 Find the maximum power transferred to resistor R in the circuit of Fig. 4.135.

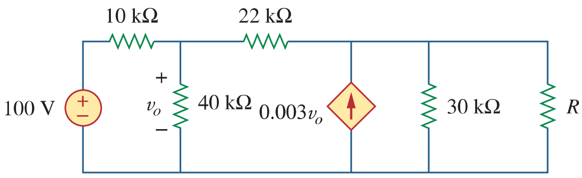

Figure 4.135
For Prob. 4.69.

4.70 Determine the maximum power delivered to the variable resistor R shown in the circuit of Fig. 4.136.

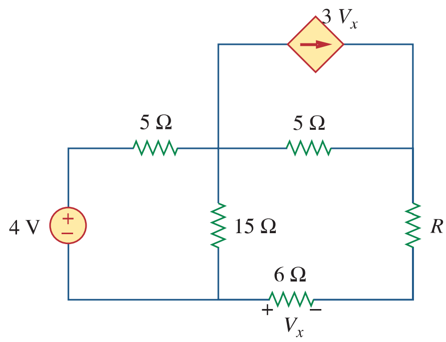

Figure 4.136
For Prob. 4.70.

4.71 For the circuit in Fig. 4.137, what resistor connected across terminals *a-b* will absorb maximum power from the circuit? What is that power?

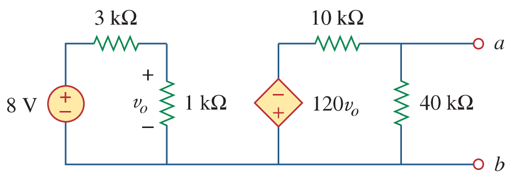

Figure 4.137
For Prob. 4.71.

4.72 (a) For the circuit in Fig. 4.138, obtain the Thevenin equivalent at terminals *a-b*.
(b) Calculate the current in $R_L = 8\ \Omega$.
(c) Find R_L for maximum power deliverable to R_L.
(d) Determine that maximum power.

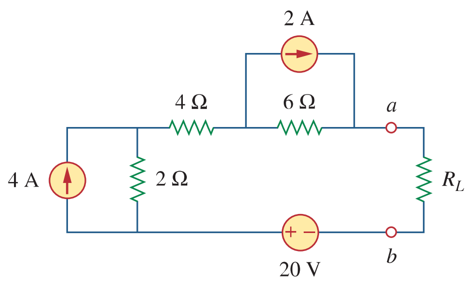

Figure 4.138
For Prob. 4.72.

4.73 Determine the maximum power that can be delivered to the variable resistor R in the circuit of Fig. 4.139.

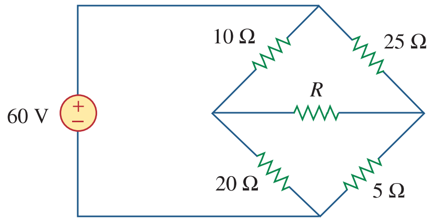

Figure 4.139
For Prob. 4.73.

4.74 For the bridge circuit shown in Fig. 4.140, find the load R_L for maximum power transfer and the maximum power absorbed by the load.

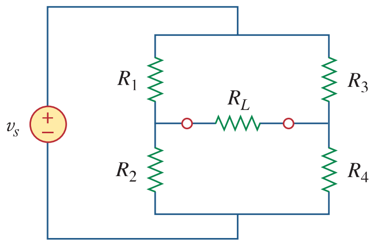

Figure 4.140
For Prob. 4.74.

***4.75** For the circuit in Fig. 4.141, determine the value of R such that the maximum power delivered to the load is 3 mW.

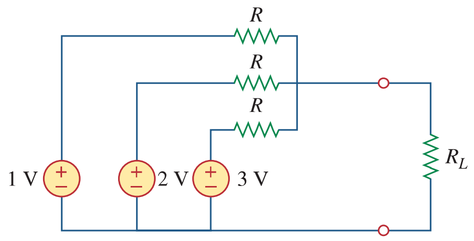

Figure 4.141
For Prob. 4.75.

Section 4.9 Verifying Circuit Theorems with *PSpice*

4.76 Solve Prob. 4.34 using *PSpice or MultiSim*. Let $V = 40$ V, $I = 3$ A, $R_1 = 10\ \Omega$, $R_2 = 40\ \Omega$, and $R_3 = 20\ \Omega$.

4.77 Use *PSpice or MultiSim* to solve Prob. 4.44.

4.78 Use *PSpice or MultiSim* to solve Prob. 4.52.

4.79 Obtain the Thevenin equivalent of the circuit in Fig. 4.123 using *PSpice or MultiSim*.

4.80 Use *PSpice or MultiSim* to find the Thevenin equivalent circuit at terminals *a-b* of the circuit in Fig. 4.125.

4.81 For the circuit in Fig. 4.126, use *PSpice or MultiSim* to find the Thevenin equivalent at terminals *a-b*.

Section 4.10 Applications

4.82 A battery has a short-circuit current of 20 A and an open-circuit voltage of 12 V. If the battery is connected to an electric bulb of resistance 2 Ω, calculate the power dissipated by the bulb.

4.83 The following results were obtained from measurements taken between the two terminals of a resistive network.

Terminal Voltage	12 V	0 V
Terminal Current	0 A	1.5 A

Find the Thevenin equivalent of the network.

4.84 When connected to a 4-Ω resistor, a battery has a terminal voltage of 10.8 V but produces 12 V on an open circuit. Determine the Thevenin equivalent circuit for the battery.

4.85 The Thevenin equivalent at terminals *a-b* of the linear network shown in Fig. 4.142 is to be determined by measurement. When a 10-kΩ resistor is connected to terminals *a-b*, the voltage V_{ab} is measured as 6 V. When a 30-kΩ resistor is connected to the terminals, V_{ab} is measured as 12 V. Determine: (a) the Thevenin equivalent at terminals *a-b*, (b) V_{ab} when a 20-kΩ resistor is connected to terminals *a-b*.

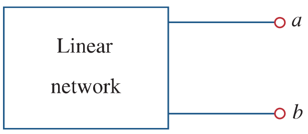

Figure 4.142
For Prob. 4.85.

4.86 A black box with a circuit in it is connected to a variable resistor. An ideal ammeter (with zero resistance) and an ideal voltmeter (with infinite resistance) are used to measure current and voltage as shown in Fig. 4.143. The results are shown in the table on the next page.

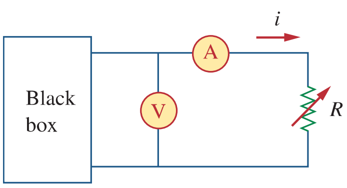

Figure 4.143
For Prob. 4.86.

(a) Find i when $R = 4\ \Omega$.

(b) Determine the maximum power from the box.

$R(\Omega)$	V(V)	i(A)
2	3	1.5
8	8	1.0
14	10.5	0.75

4.87 A transducer is modeled with a current source I_s and a parallel resistance R_s. The current at the terminals of the source is measured to be 9.975 mA when an ammeter with an internal resistance of 20 Ω is used.

(a) If adding a 2-kΩ resistor across the source terminals causes the ammeter reading to fall to 9.876 mA, calculate I_s and R_s.

(b) What will the ammeter reading be if the resistance between the source terminals is changed to 4 kΩ?

4.88 Consider the circuit in Fig. 4.144. An ammeter with internal resistance R_i is inserted between A and B to measure I_o. Determine the reading of the ammeter if: (a) $R_i = 500\ \Omega$, (b) $R_i = 0\ \Omega$. (*Hint*: Find the Thevenin equivalent circuit at terminals *a*-*b*.)

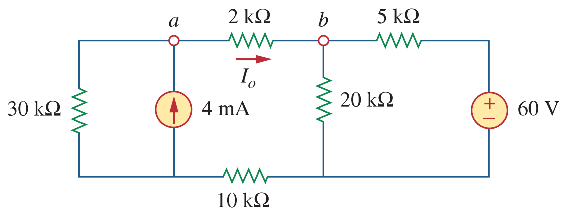

Figure 4.144
For Prob. 4.88.

4.89 Consider the circuit in Fig. 4.145. (a) Replace the resistor R_L by a zero resistance ammeter and determine the ammeter reading. (b) To verify the reciprocity theorem, interchange the ammeter and the 12-V source and determine the ammeter reading again.

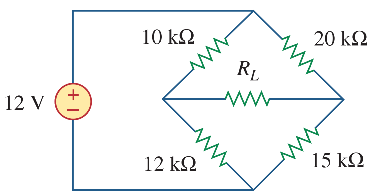

Figure 4.145
For Prob. 4.89.

4.90 The Wheatstone bridge circuit shown in Fig. 4.146 is used to measure the resistance of a strain gauge. The adjustable resistor has a linear taper with a maximum value of 100 Ω. If the resistance of the strain gauge is found to be 42.6 Ω, what fraction of the full slider travel is the slider when the bridge is balanced?

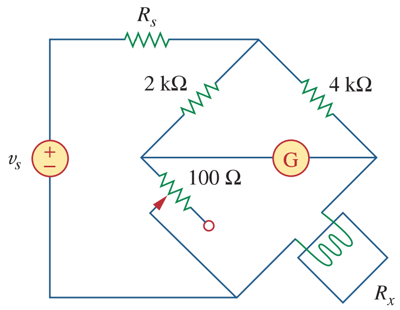

Figure 4.146
For Prob. 4.90.

4.91 (a) In the Wheatstone bridge circuit of Fig. 4.147, select the values of R_1 and R_3 such that the bridge can measure R_x in the range of 0–10 Ω.

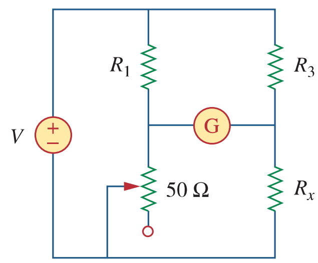

Figure 4.147
For Prob. 4.91.

(b) Repeat for the range of 0–100 Ω.

***4.92** Consider the bridge circuit of Fig. 4.148. Is the bridge balanced? If the 10-kΩ resistor is replaced by an 18-kΩ resistor, what resistor connected between terminals *a*-*b* absorbs the maximum power? What is this power?

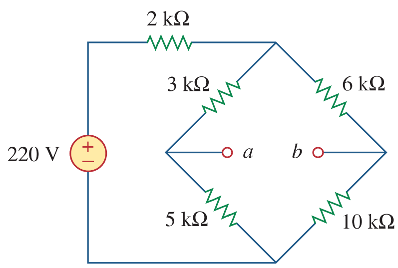

Figure 4.148
For Prob. 4.92.

Comprehensive Problems

4.93 The circuit in Fig. 4.149 models a common-emitter transistor amplifier. Find i_x using source transformation.

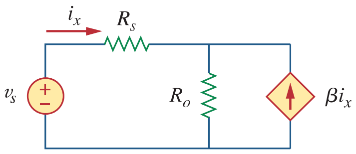

Figure 4.149
For Prob. 4.93.

4.94 An attenuator is an interface circuit that reduces the voltage level without changing the output resistance.

(a) By specifying R_s and R_p of the interface circuit in Fig. 4.150, design an attenuator that will meet the following requirements:

$$\frac{V_o}{V_g} = 0.125, \qquad R_{eq} = R_{Th} = R_g = 100\ \Omega$$

(b) Using the interface designed in part (a), calculate the current through a load of $R_L = 50\ \Omega$ when $V_g = 12$ V.

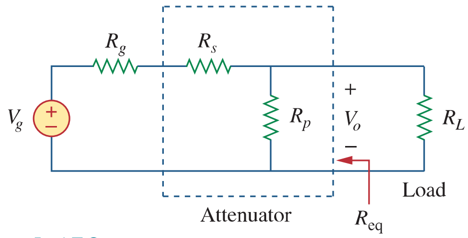

Figure 4.150
For Prob. 4.94.

***4.95** A dc voltmeter with a sensitivity of 20 kΩ/V is used to find the Thevenin equivalent of a linear network. Readings on two scales are as follows:

(a) 0–10 V scale: 4 V (b) 0–50 V scale: 5 V

Obtain the Thevenin voltage and the Thevenin resistance of the network.

***4.96** A resistance array is connected to a load resistor R and a 9-V battery as shown in Fig. 4.151.

(a) Find the value of R such that $V_o = 1.8$ V.

(b) Calculate the value of R that will draw the maximum current. What is the maximum current?

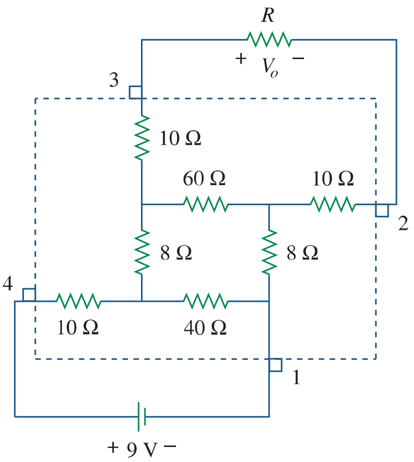

Figure 4.151
For Prob. 4.96.

4.97 A common-emitter amplifier circuit is shown in Fig. 4.152. Obtain the Thevenin equivalent to the left of points B and E.

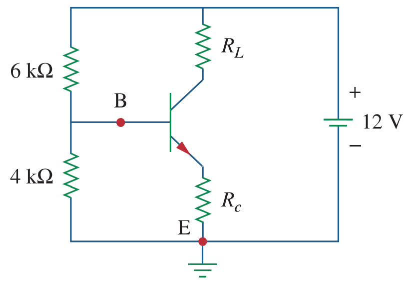

Figure 4.152
For Prob. 4.97.

***4.98** For Practice Prob. 4.18, determine the current through the 40-Ω resistor and the power dissipated by the resistor.