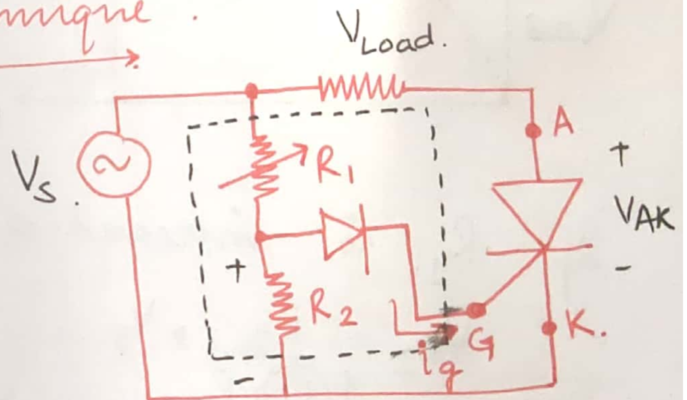
SCR triggering techniques

SCR can be triggered/ latched into conduction in many ways:-

1) Break Over (not practised).
2) dv/dt (unwanted)
3) Thermal triggering
4) Light triggering (LASCR's in HVDC systems).
5) Gate triggering (through gate pulse).
   ↳ most common triggering technique.

Gate Triggering of SCRs.

1) Resistance triggering technique.



* **Power ckt :-**

$V_S = V_{Load} + V_{SCR}$.

When SCR is ON,

$V_{SCR} = 0$, $V_s = V_{Load}$.

When SCR is OFF,
all applied voltage across SCR.

$V_{SCR} = V_{AK} = V_s$.

[Diode prevents reverse flow of i_g as -ve i_g is useless].

* **Gate Ckt :-**

$V_s = V_{R_1} + V_{R_2}$.

'i_g' is to be controlled.
↳ depends on 'V_{R_2}' drop ⇒ $V_{R_2} \uparrow \Rightarrow i_g \uparrow$.

$V_{R_2} = \frac{R_2}{R_1 + R_2} \times V_s$ → A.C varies with time.

R_1 → variable

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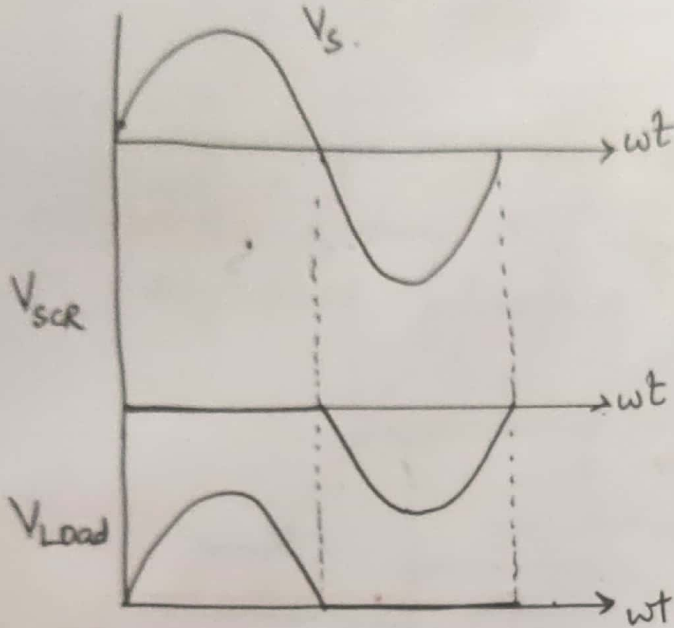
Now if R_1 is small

⇒ V_{R_2} is high

⇒ i_g ↑ even if V_s is small.

⇒ SCR triggers.

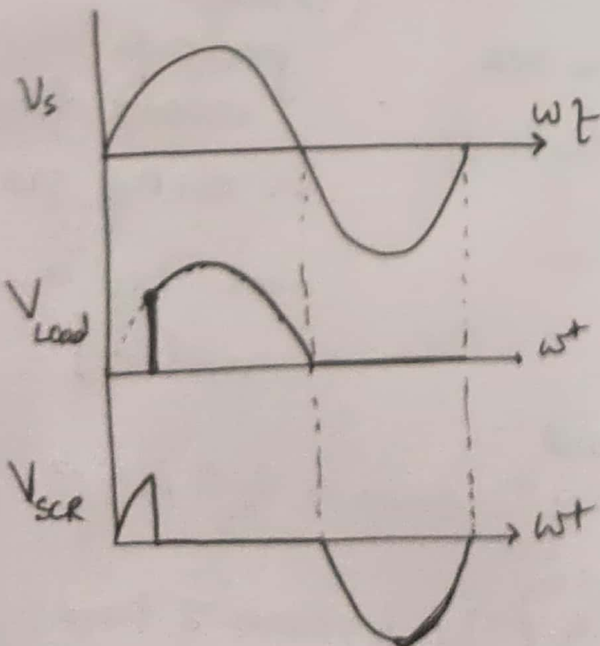


If R_1 is increased ⇒

$$V_{R_2} = \frac{R_2}{\uparrow R_1 + R_2} \times V_s$$

As R_1 is increased, V_{R_2} reduces & the SCR waits for the souce voltage to increase, so that V_{R_2} may increase & then the SCR triggers.

This delay from zero crossing is called firing angle α.



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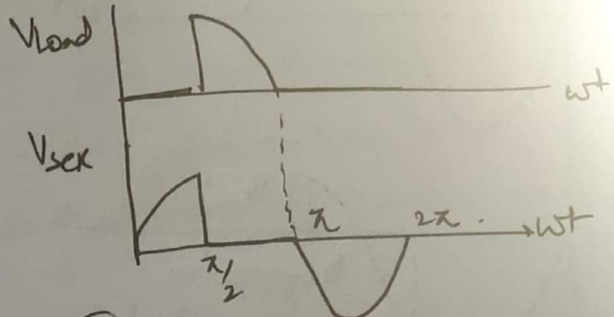
Now, if $R_1 \uparrow\uparrow$ ~~until~~ ⇒ $\alpha \uparrow$ goes on increase

till $\alpha = 90°$



But beyond $\alpha = 90°$,
if we further ~~incr~~ increase R_1.

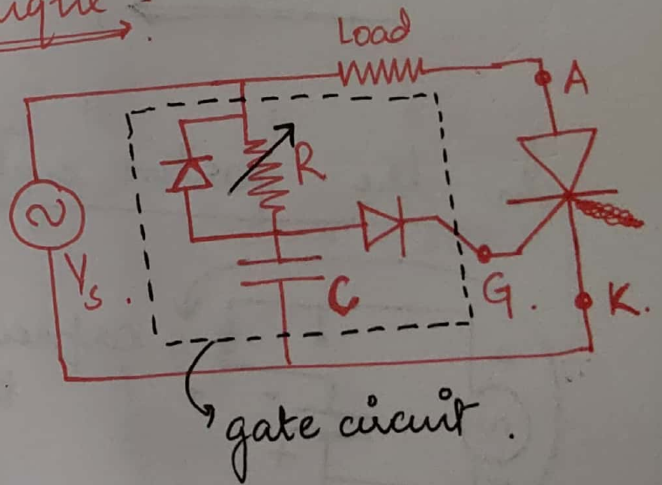
⇒ $V_{R_2} = \frac{R_2}{\uparrow\uparrow R_1 + R_2}$ ↓↓↓ $\propto V_s$ → itself falls after 90°.
∴ conduction not possible.

Limitations of R triggering

1) continuous gate signal.
   ↳ resistances involved / hence losses.

2) firing angle control from 0 to 90°.

2). RC triggering technique:-



* Power ckt.

$V_s = V_{Load} + V_{AK}$

when SCR is ON.

$V_{AK} = 0$.

$\boxed{V_s = V_{Load}}$

when SCR is OFF ⇒ $V_s = V_{AK}$

and $\boxed{V_{Load} = 0}$

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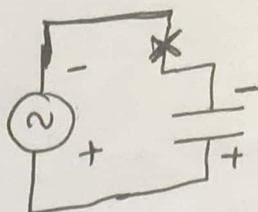
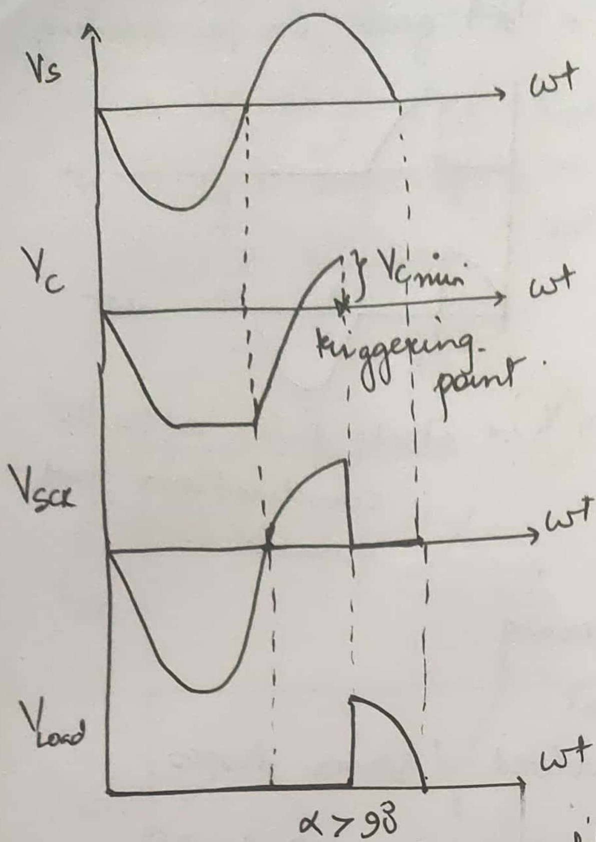
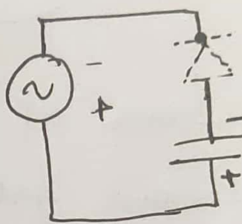
In the negative cycle ⟹



Until V_c acquires peak -ive voltage.



After $\pi/2$



V_c acquires high magnitude & V_s falls.

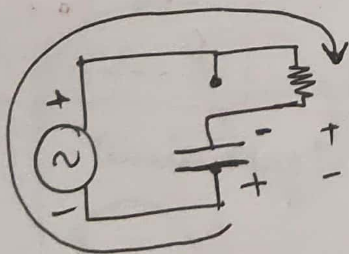
→ Diode reverse biased by capacitor.

also possible ⟹

α = 0 to 180° is possible ⟶

Capacitor maintains ~~gradually~~ $-V_c$ ~~loss~~.

In the positive cycle ⟶



capacitor discharges through resistor. hence losing potential. & gaining +ive potential in steady state.

until $V_c = V_{gmin}$

↳ enough to trigger SCR ⟶ 0 to 180°

Inefficient method → Continuous gate current.

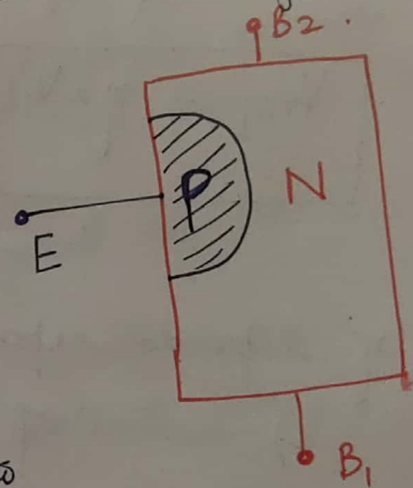
3) Pulse Gate triggering:

A gate pulse (momentary) is issued into the gate-{cathode} terminals of SCR, preventing losses that are otherwise associated with continuous gate triggering.

↳ UNI-JUNCTION TRANSISTOR. (UJT).

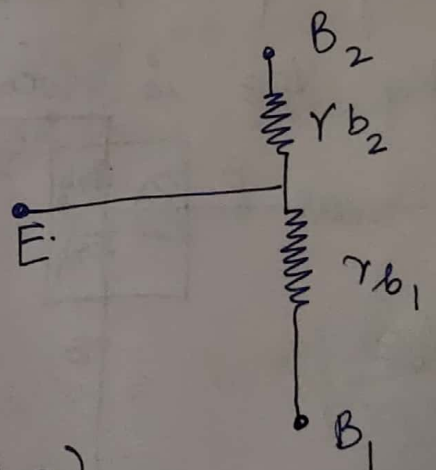
↳ used to generate firing pulses for an SCR.

* A P-type region is diffused onto an N-type region.
* P region is heavily doped.
* N region is lightly doped.
* P region is diffused closer to Base B_2.



* Inter-base resistance R_{BB} is high due to lightly doped 'N' region. ⟷ (4-10kΩ)

Equivalent ckt

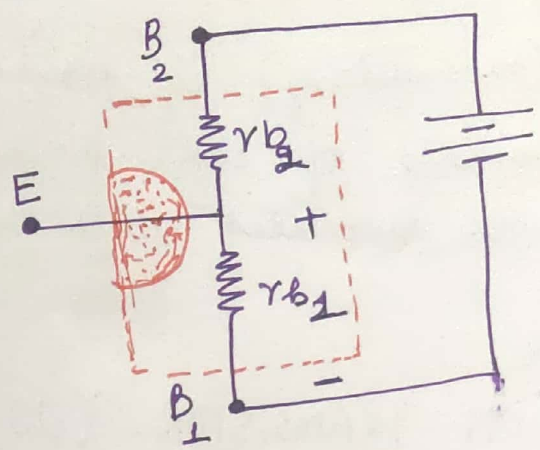


Since E is closer to B_2, $rb_2 < rb_1$

$R_{BB} = rb_1 + rb_2$ (kΩ).

↳ inter base resistance.

Now, assume a supply voltage given to the UJT,



$$V_{rb_1} = V_A = \left(\frac{rb_1}{rb_1 + rb_2}\right) \times V_s$$

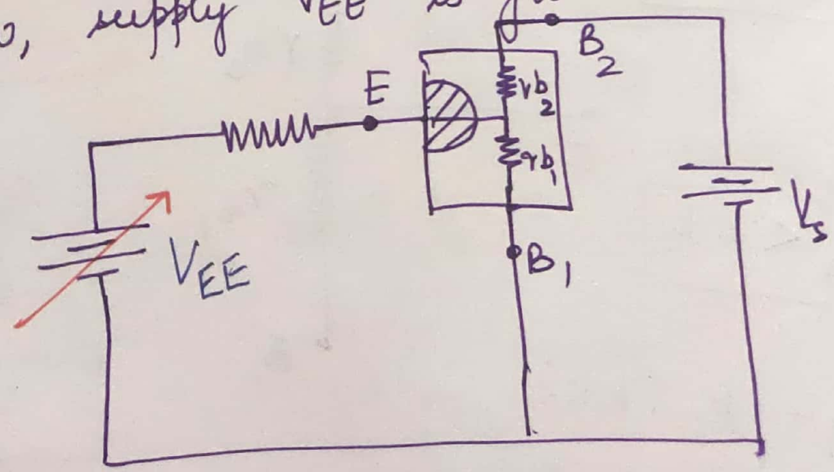
$$\boxed{V_{rb_1} = \eta \times V_s}$$ ⇒ where 'η' is intrinsic stand-off ratio.

'η' depends upon:→

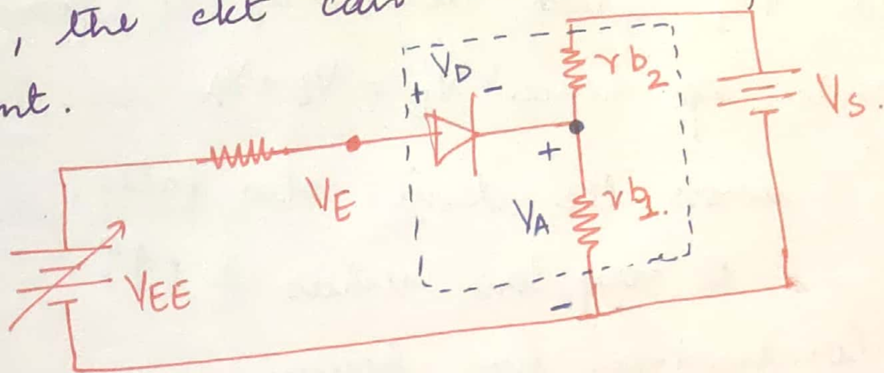
1) nature of material / doping levels.
2) spacing of emitter b/w the 2 bases

Usually η is b/w 0.5 to 0.8.

Now, supply V_{EE} is given



Assuming the PN junction to emulate a diode, the ckt can have the following equivalent.



When device is OFF

$V_{EE} = V_E = V_D + V_A$.

If applied voltage

$V_E < V_D + V_A$ ↳ junction potential not overcome.

↓

reverse biased condition.

↳ voltage being blocked by UJT.

Now, as V_{EE} increases (i.e we increase applied voltage).

↳ The potential barrier is overcome.

↳ holes injected from P region to N region along rb_1 path.

⇒ carrier concentration around rb_1 region increases. ⇒ resistance rb_1 rapidly starts to fall.

As rb_1 falls ⇒ $V_A = \left[\frac{rb_1}{rb_1 + rb_2} \times V_s \right]$ also falls.

i.e $V_{EE} > V_D + V_A$ ⇒ stronger ~~F~~B.

$i \uparrow\uparrow$.

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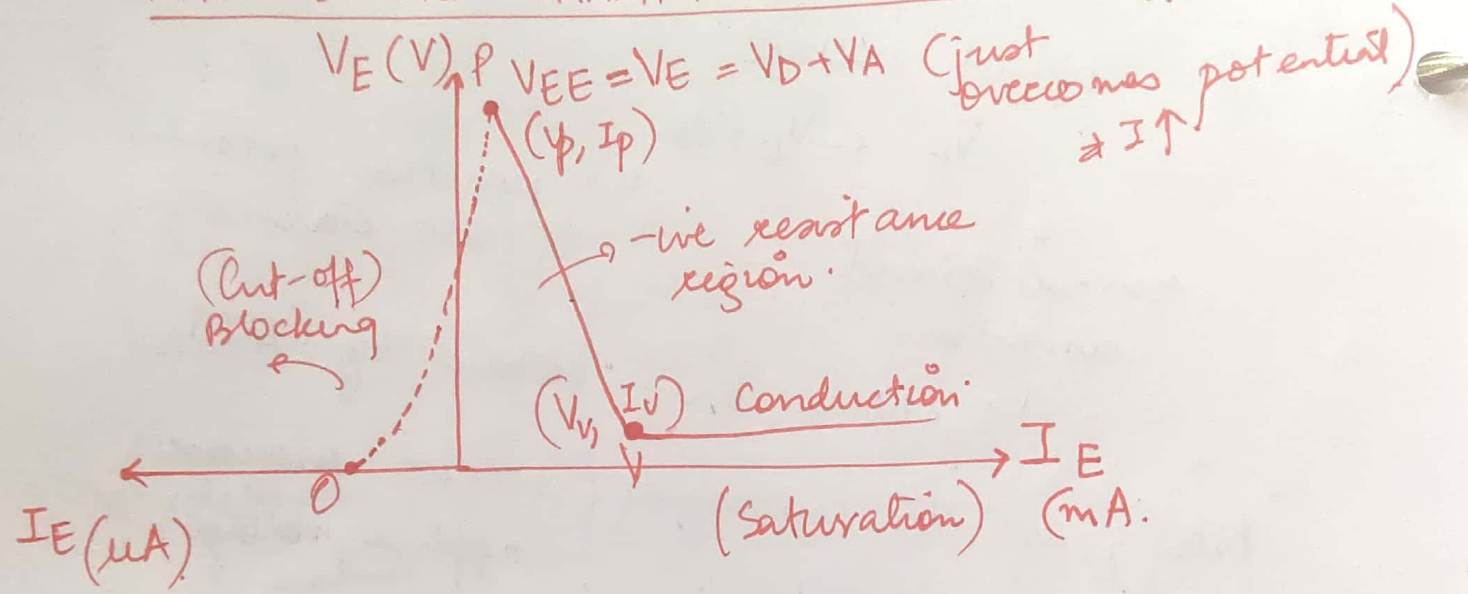
→ cumulative process.
until r_{b_1} falls drastically. (from k-Ω to Ω).
and ~~op~~ hence $V_E = V_D + V_A$
across the device also falls
to very low values. & I↑↑.
↳ Conduction has begun.

STATIC-EMITTER CHARACTERISTICS OF UJT.



OP → Blocking interval
→ OFF → UJT blocks all voltage, carries only leakage currents.

At P,
applied F.B just overcomes potential barrier, device goes into conduction.
(transits into conduction)
through -ive resistance region (V↓, I↑)
(P to V)

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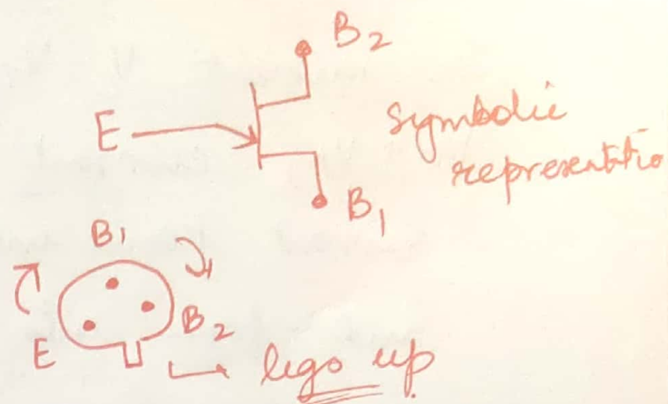
After V, device has reached a steady state conduction period.

minimum Voltage V_V attained.

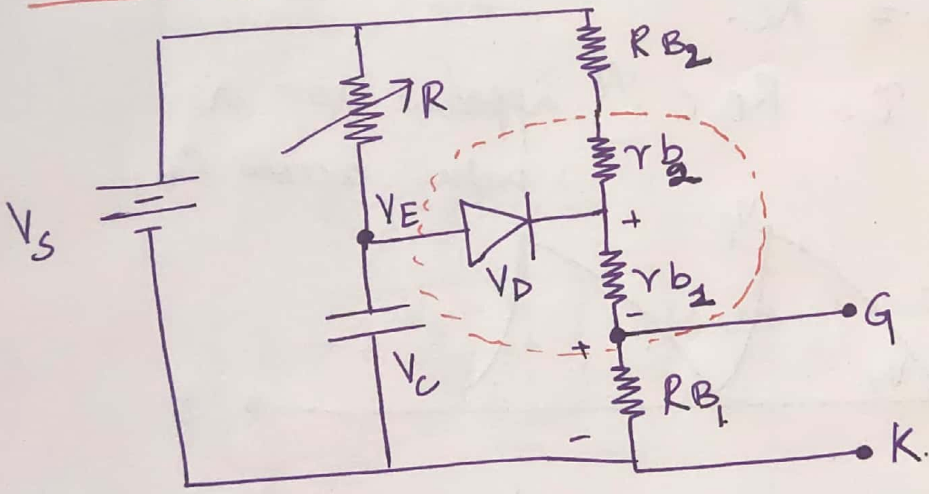
P → Peak point,

V → Valley point,



UJT as a relaxation Oscillator

How to generate firing pulses using UJT?



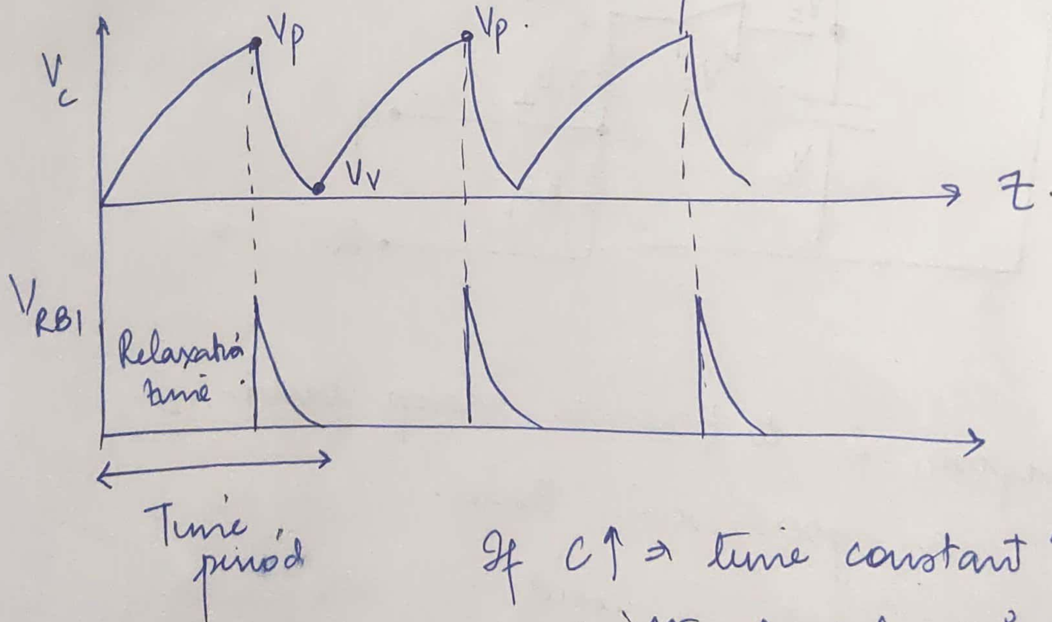
Purpose is to generate sharp pulse with a good rise time.

Only one supply is needed.
↳ V_s

The same V_A develop potential V_A across UJT, and the same V_A also charges V_C through R & V_C starts rising.

The moment $V_C = V_Z$ overcomes potential barrier $V_D + V_A$, current injection begins. current flows into rb_1 region ($rb_1 \downarrow\downarrow$) and hence into R_{B_1} too, producing a sharp pulse determined by discharge of capacitor through R_{B_1} resistor.

Charging $\tau = RC$.
Discharging $\tau = R_{B_1}C$. } appears as a pulse across R_{B_1}.



If $C\uparrow \Rightarrow$ time constant $\uparrow$. width of pulse is increase to ensure successful triggering of SCR beyond latching

Typical values.

$R_{B_1} \leq 100\Omega$

$R_{B_2} > 100\Omega$

$V_s = 10-35V.$

for successful triggering

↳ turn ON of UJT

* current to flow.

* V_{GK} to appear on SCR terminals.

$$V_c > V_p.$$

$$V_s - I_p R > V_p.$$

$$R < \frac{V_s - V_p}{I_p}$$ → upper limit of R.

For UJT to successfully be able to go off when V_c falls below V_v.

$$V_c < V_v.$$

$$V_s - I_v R < V_v.$$

$$R > \frac{V_s - V_v}{I_v}$$ lower limit of R.

$$\therefore \frac{V_s - V_v}{I_v} < R < \frac{V_s - V_p}{I_p}$$

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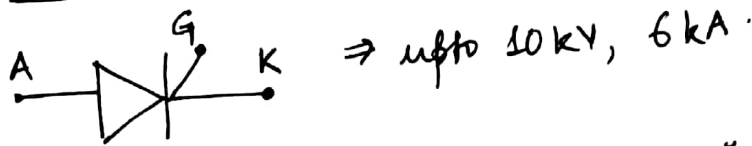
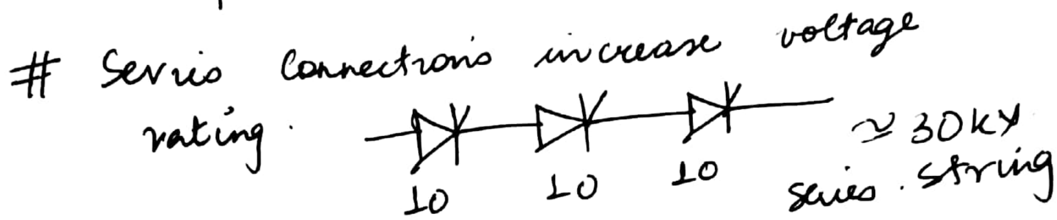
MULTIPLE CONNECTIONS OF SCRs

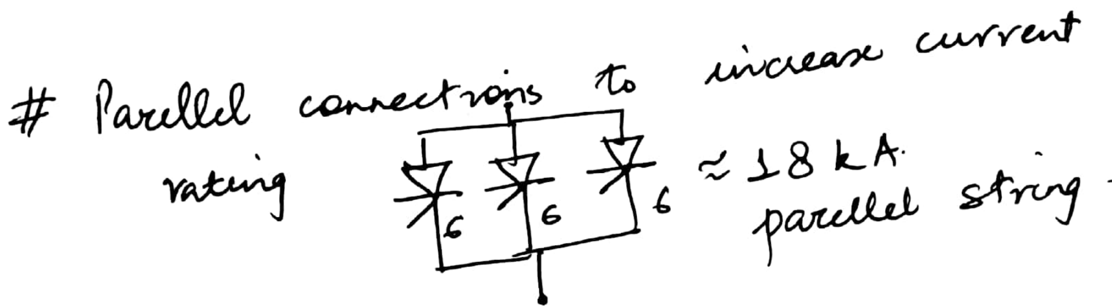


⇒ upto 10 kV, 6 kA.

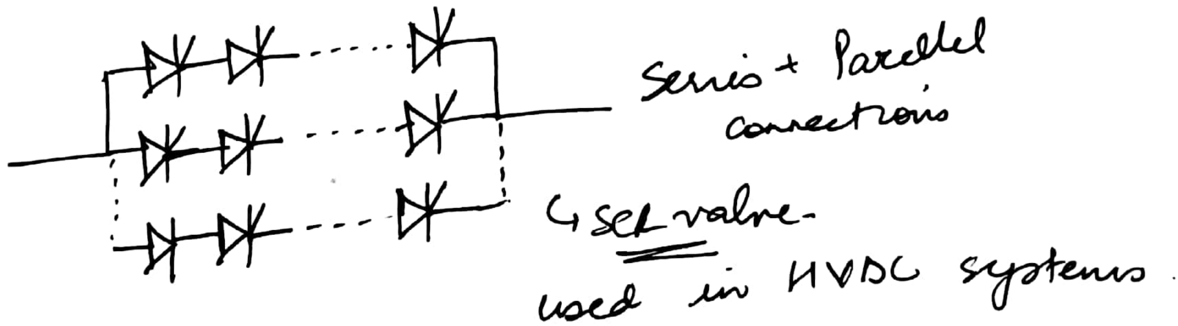
In higher ratings SCR applications, multiple connections of SCRs are done.



Series connections increase voltage rating. ≃ 30 kV series string



Parallel connections to increase current rating ≃ 18 kA parallel string.



Series + Parallel connections

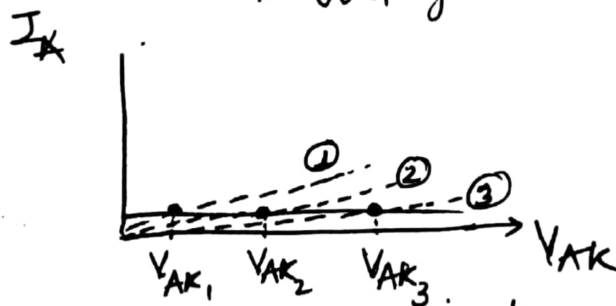
↳ SCR valve.

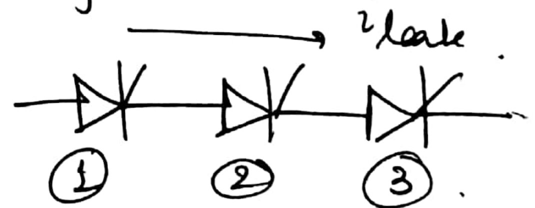
used in HVDC systems.

Problem in Series Connections

Series ⇒ Voltage sharing

↳ voltage blocking mode.





↳ resistances offered by three SCRs are different.

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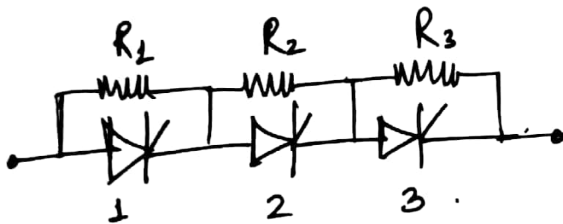
Due to small shift in static VI characteristics, unequal voltage sharing may take place.
In case the voltage shared by any one of the SCRs exceeds its V_{BO}, unwanted conduction might happen. Breakdown may also happen if rating is exceeded.

Solⁿ :→

Connect Resistances in shunt.



$R_{SCR_1} \parallel R_1$

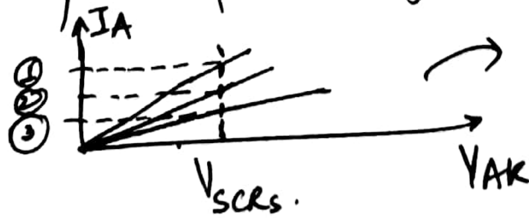
$= R_{SCR_2} \parallel R_2$

$= R_{SCR_3} \parallel R_3$.

(1) Effective resistances are equalized.

↳ Characteristics are made to overlap.

(2) Another aspect of seeing the same thing



→ individual currents in SCRs are different but voltage sharing is same.

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It might be difficult to design separate resistances R_1, R_2, R_3 and a single equalizing resistance may be connected → R_E.

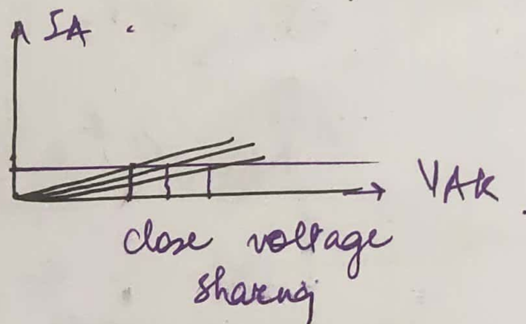
such that $R_E >>>$ individual SCR resistances.

10k, 20k, 30k → SCR_1, SCR_2, SCR_3.

RE = 100k.

9.09kΩ, 16.67kΩ, 23.07kΩ

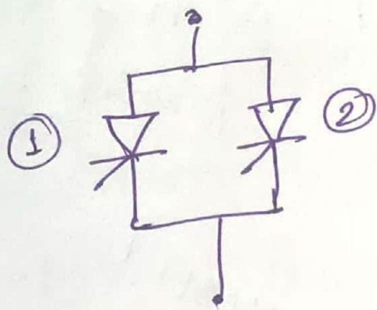
9.6kΩ. ↳ difference is reduced.

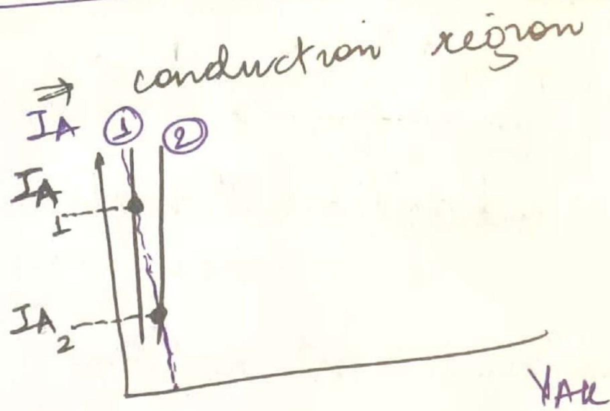


close voltage sharing

↳ won't exceed Break Over voltage for any SCR.

Problems in parallel connections :

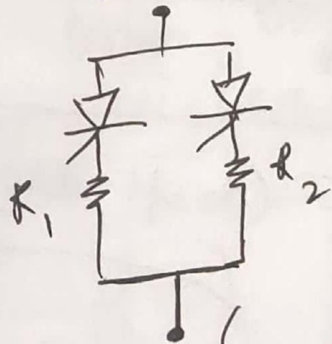




Unequal resistances exhibited during conduction.
↳ same V_{AK} & unequal currents.

The SCR carrying higher current heats up & carriers ↑ & resistance ↓.
& draws more current.
⇒ works in positive feedback until SCR burns.

Sol^n (1) :→

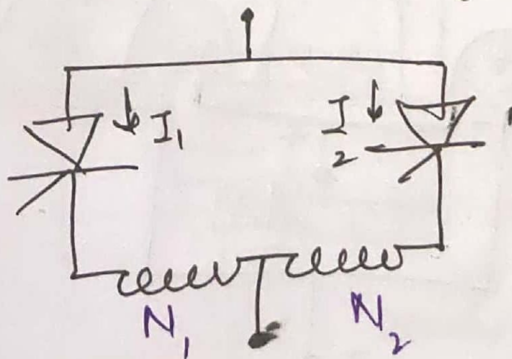


$SCR_1 + R_1 = SCR_2 + R_2$.

⇒ Equalized resistance.

↳ lossy bad idea.

Sol^n (2)



$N_1 I_1 = N_2 I_2$.

If I_1 ↑.
↳ $N_1 I_1$ ↑.
↳ voltage induced such that I_1 is reduced.

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POWER MOSFETS

$S\,(n^+ p n^- n^+)$ structure - D

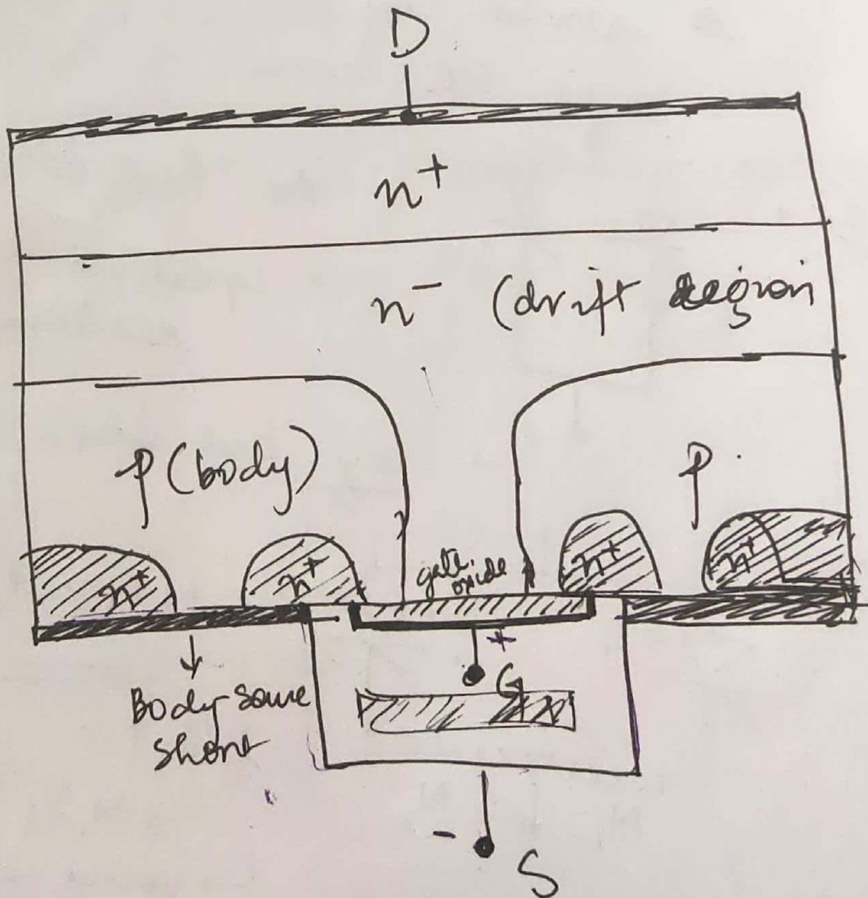
$\{ n^+ n^- p\, n^+ \}$ from D to S

↳ enhancement mode 'n' channel mosfet.

Two extreme n^+ regions are highly doped

The intermediate 'p' region (→ body of MOSFET) serves as a chanel b/w D & S.

& n^- region is the drain drift region that determines break down voltage. (depletion layer penetrates here)



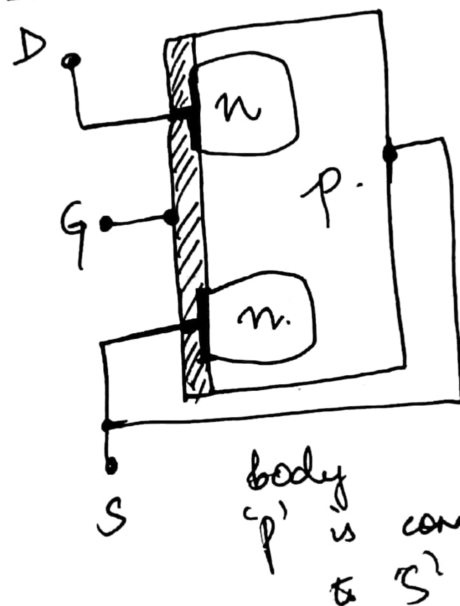
At first it appears, no current flow is possible because one of the 2 junctions (Drain-Body / Body-Source) will always be reversed biased irrespective of applied V_{DS} polarity.

* Also minority carriers injection from gate to body (source) is not possible because of insulation b/w gate & body through gate oxide.

However, if V_{GS} (+ve) is given, it creates an n-channel beneath the gate oxide. hence connecting S to D

⟶ Boylestad ⟹

npn MOSFET (n-channel MOSFET).



enhancement type ⇒ no physical channel is present

V_{DS} +ve or -ve (One of the 2 junctions will be reverse biased).

body 'p' is connected to 'S'?

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When V_{DS} is +ive (Saturation)

but a +ive V_{GS} is also given:

majority carriers of p region (holes) start moving away from the gate leaving -ve charge near G

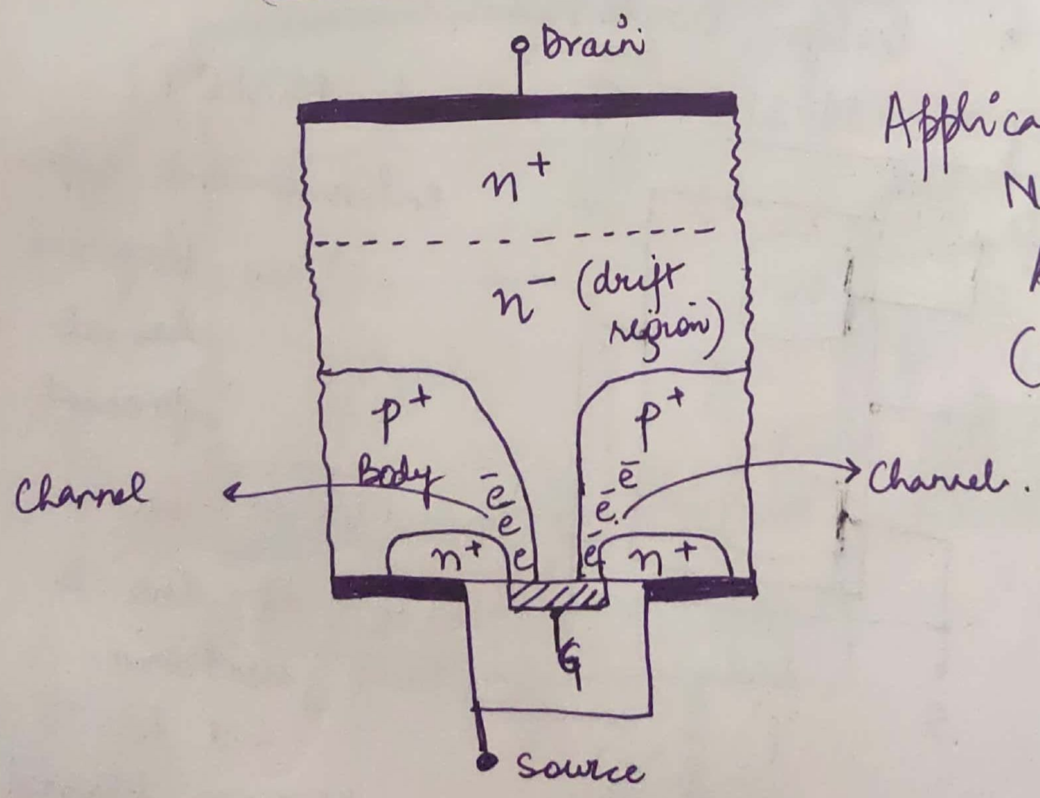
and minority carriers of p region (e's) start moving closer to gate

As a result, a negative chanel is established b/w D & S to facilitate flow of current

For MOSFETs in the power range, structural modifications are made.

1) Vertically mounted

2) Additional (n^-) layer.

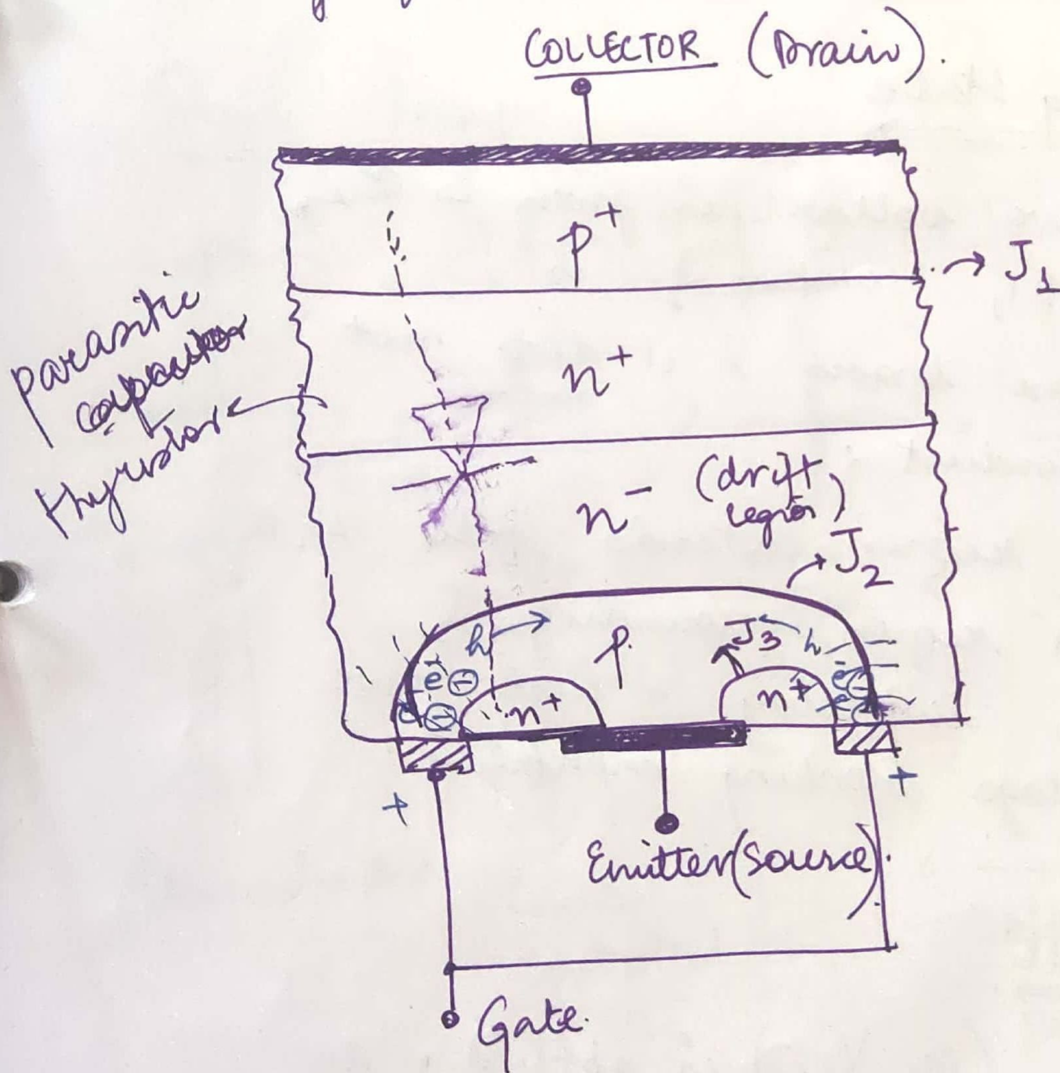


Application Note AN-1084. (Internation Rectifier)

It is a voltage controlled device, ... by V_{GE}.

Available in higher ratings as compared to Power MOSFET

switching frequency less than Power MOSFET. (20 kHz).



Turn ON of parasitic thyristor should be avoided in the operation of IGBT.

↳ This is prevented by means of the source-body short.

Physics of Device Operation

Blocking state

When +ve voltage is given to the IGBT, junction J_2 is reverse biased & it does not conduct.

→ Depletion region extends into n^- region surrounding J_2 hence imparting a high +ve voltage blocking capability.

ON STATE:

When V_{GE} (or V_{GS}) is applied, an inversion layer forms beneath the gate

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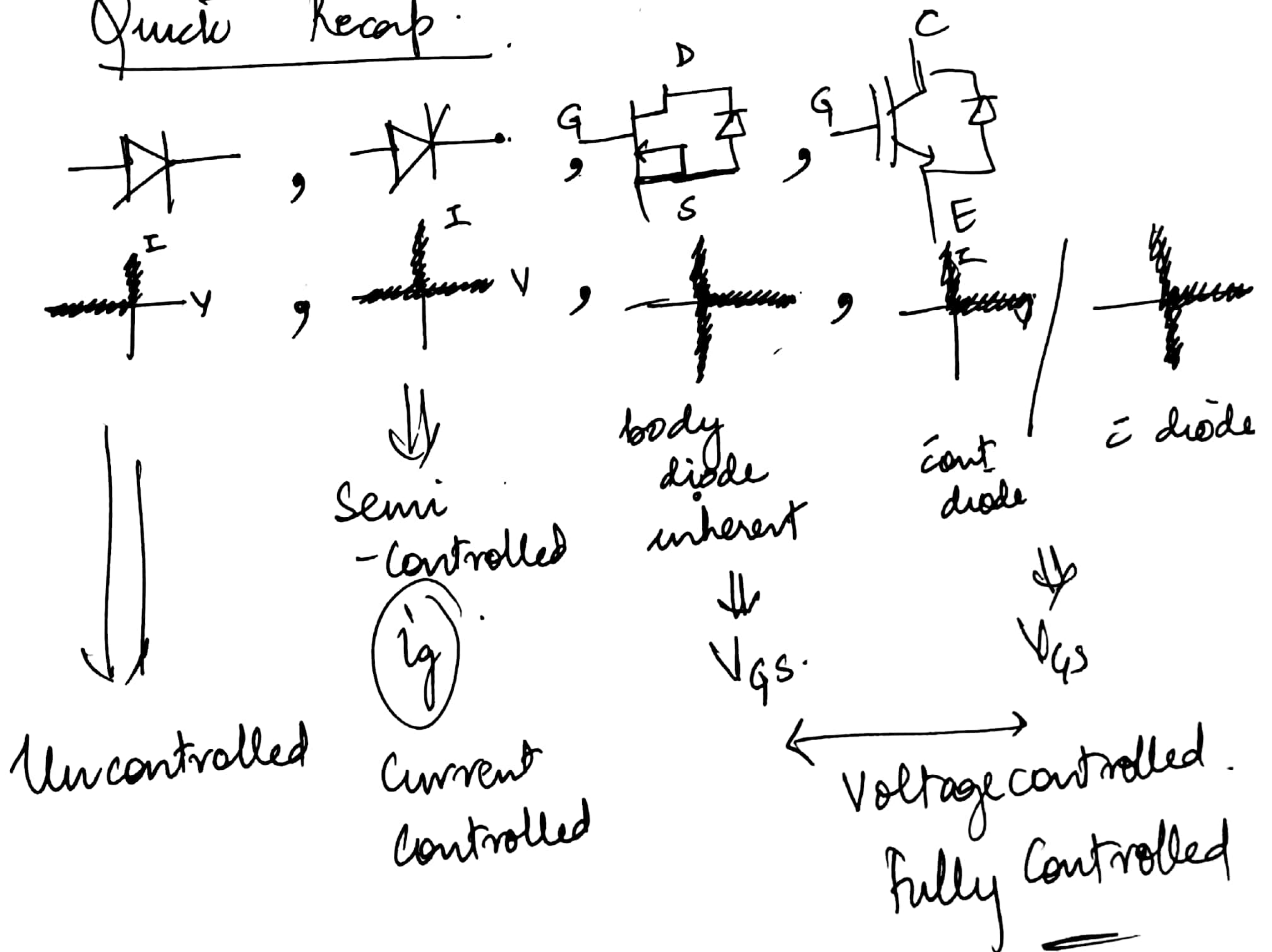
This layers shorts the two 'n' regions (n^- with n^+) just as in a MOSFET.

⇒ current flows through this inversion layer (or channel) hence resulting in significant (hole) → carrier injection from p^+ (drain/collector) to n^+ (source/emitter).

Quick Recap.



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